

SN54ALS113A, SN74ALS113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

SDAS200 – D2661, APRIL 1982 – REVISED MAY 1986

- Fully Buffered to Offer Maximum isolation from External Disturbance
- Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS113A	40 MHz ($C_L=15$ pF)	6 mW

description

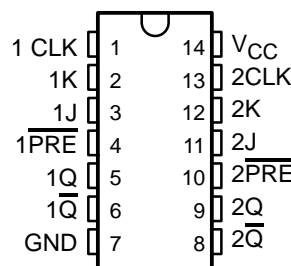
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset \overline{PRE} is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS113A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS113A is characterized for operation from 0°C to 70°C .

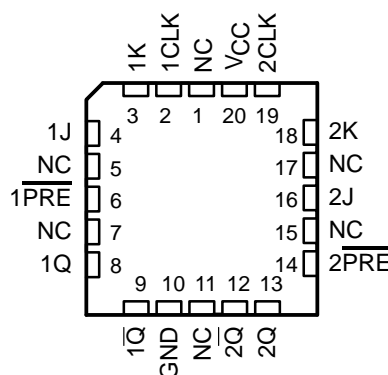
FUNCTION TABLE

INPUTS				OUTPUTS	
\overline{PRE}	CLK	J	K	Q	\overline{Q}
L	X	X	X	H	L
H	\downarrow	L	L	Q_0	\overline{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	TOGGLE
H	H	X	X	Q_0	\overline{Q}_0

SN54ALS113A . . . J PACKAGE
SN74ALS113A . . . D OR N PACKAGE
(TOP VIEW)

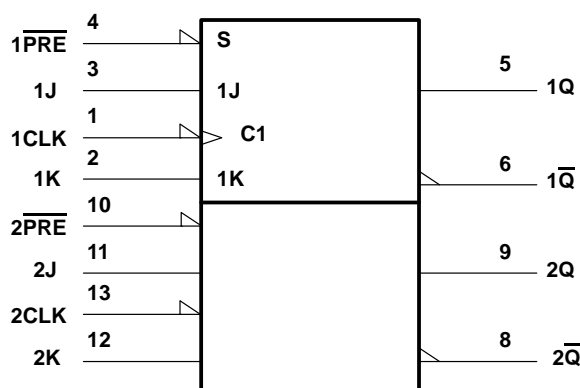


SN54ALS113A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

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The diagram illustrates a J-K flip-flop implemented using two 4-input multiplexers and two 4-input OR gates. The inputs are J, K, PRE (active-low), and CLK. The outputs are Q and Q-bar. The circuit uses a crossbar interconnection where the J and K inputs are connected to the data inputs of the multiplexers, and the Q and Q-bar outputs are connected to the select inputs. The PRE signal is connected to the active-low enable inputs of both multiplexers. The CLK signal is connected to the clock inputs of both multiplexers. The output of the first multiplexer is Q, and the output of the second multiplexer is Q-bar.

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS113A	-55°C to 125°C
SN74ALS113A	0°C to 70°C
Storage temperature range	-65°C to 150°C

			SN54ALS113A			SN74ALS113A			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage				0.7			0.8	V	
I _{OH}	High-level output current				−0.4			−0.4	mA	
I _{OL}	Low-level output current				4			8	mA	
f _{clock}	Clock frequency		0		25	0		30	mHz	
t _w	Pulse duration	PRE low	20			10			ns	
		CLK high	20			16.5				
		CLK low	20			16.5				
t _{su}	Setup time before CLK↓	Data	25			22			ns	
		PRE inactive	20			20				
t _h	Hold time, data after CLK↓		0			0			ns	
T _A	Operating free-air temperature		−55			125			°C	

SN54ALS113A, SN74ALS113A

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

WITH PRESET

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electrical characteristic over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS113A			SN74ALS113A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}		$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	J, K, or CLK	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$		0.1			0.1		mA
	PRE			0.2			0.2		
I_{IH}	J, K, or CLK	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$		20			20		μA
	PRE			40			40		
I_{IL}	J, K, or CLK	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.2			-0.2		mA
	PRE			-0.4			-0.4		
$I_{O\ddagger}$		$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30		-112	-30		-112	mA
I_{CC}		$V_{CC} = 5.5 \text{ V}$, See Note 1		2.5	4.5		2.5	4.5	mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				UNIT
			SN54ALS113A		SN74ALS113A		
			MIN	MAX	MIN	MAX	
f _{max}			25		30		MHz
t _{PLH}	$\overline{\text{PRE}}$	Q or $\overline{\text{Q}}$	3	23	3	14	ns
t _{PHL}			4	26	4	18	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	3	22	3	15	ns
t _{PHL}			5	23	5	19	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

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