

SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

SDLS004

D2633, JANUARY 1981—REVISED MARCH 1988

- Parallel Register Inputs ('LS592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('LS593)
- Counter has Direct Overriding Load and Clear
- Accurate Counter Frequency: DC to 20 MHz

description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive-edge-triggered clocks. In addition, the counter has direct load and clear functions. A low-going \overline{RCO} pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to CCK of the following stage.

The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs. The tables below show the operation of the enable (CCKEN, \overline{CCKEN}) inputs. A register clock enable (RCKEN) is also provided.

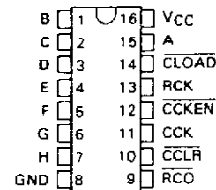
OUTPUT ENABLE CONTROL ('593 ONLY)

G	\overline{G}	A/Q _A thru H/Q _H
L	L	input mode
L	H	input mode
H	L	output mode
H	H	input mode

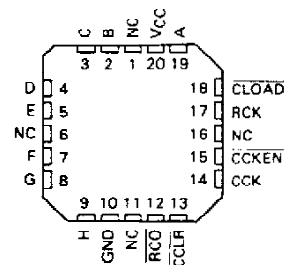
COUNTER CLOCK ENABLE CONTROL

CCKEN	\overline{CCKEN}	EFFECT ON CCK
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

SN54LS592 . . . J OR W PACKAGE SN74LS592 . . . N PACKAGE (TOP VIEW)

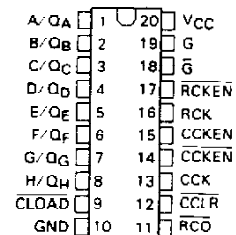


SN54LS592 . . . FK PACKAGE (TOP VIEW)

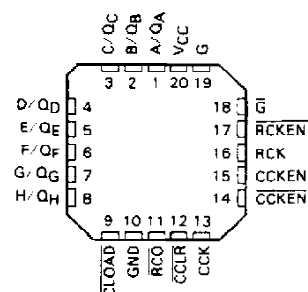


NC — No internal connection

SN54LS593 . . . J OR W PACKAGE SN74LS593 . . . DW OR N PACKAGE (TOP VIEW)



SN54LS593 . . . FK PACKAGE (TOP VIEW)



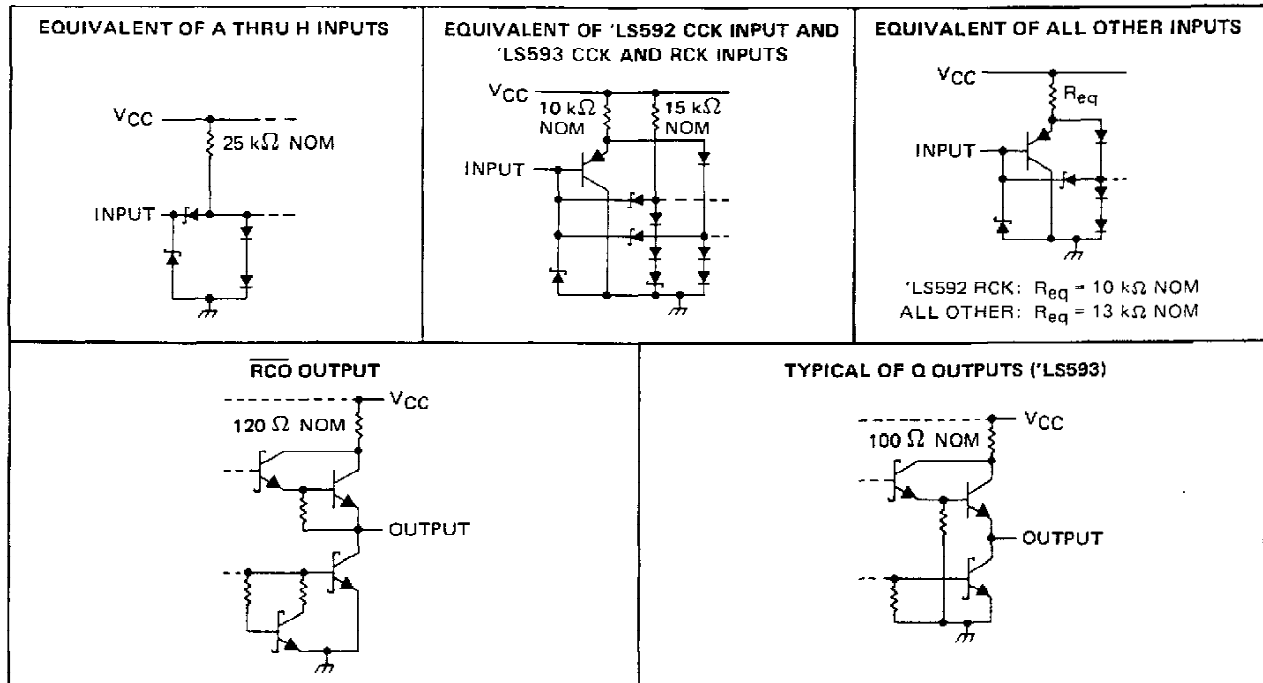
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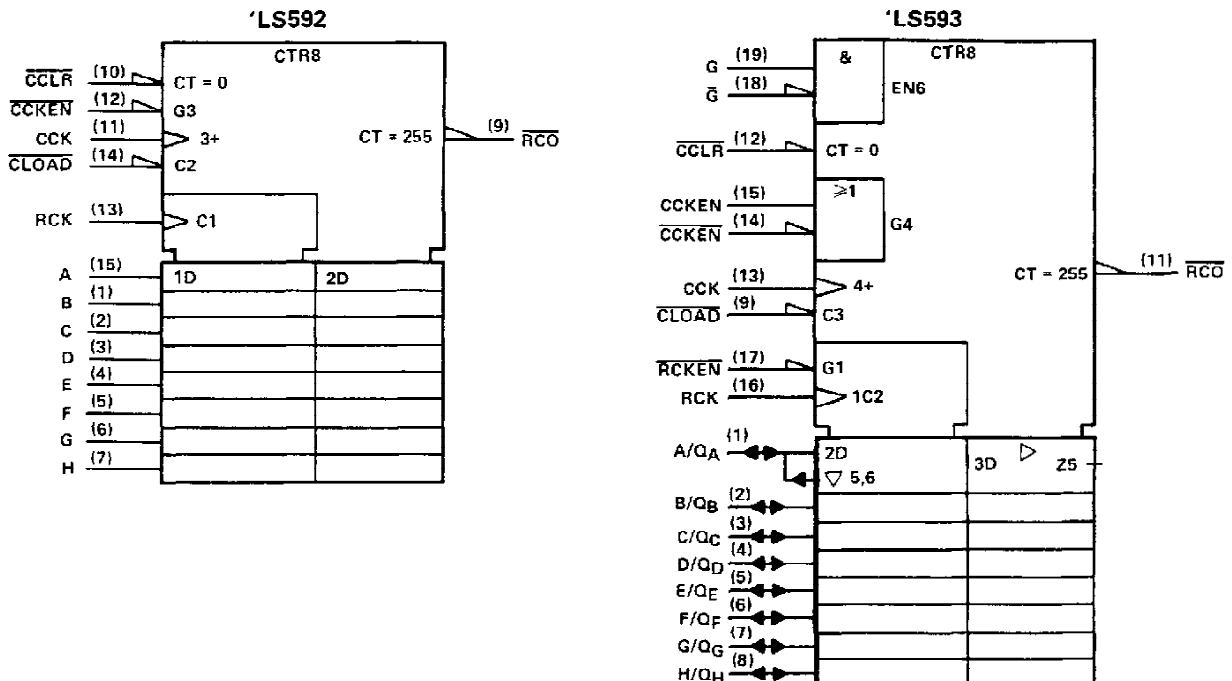
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SN54LS592, SN54LS593, SN74LS592, SN74LS593 **8-BIT BINARY COUNTERS WITH INPUT REGISTERS**

schematics of inputs and outputs



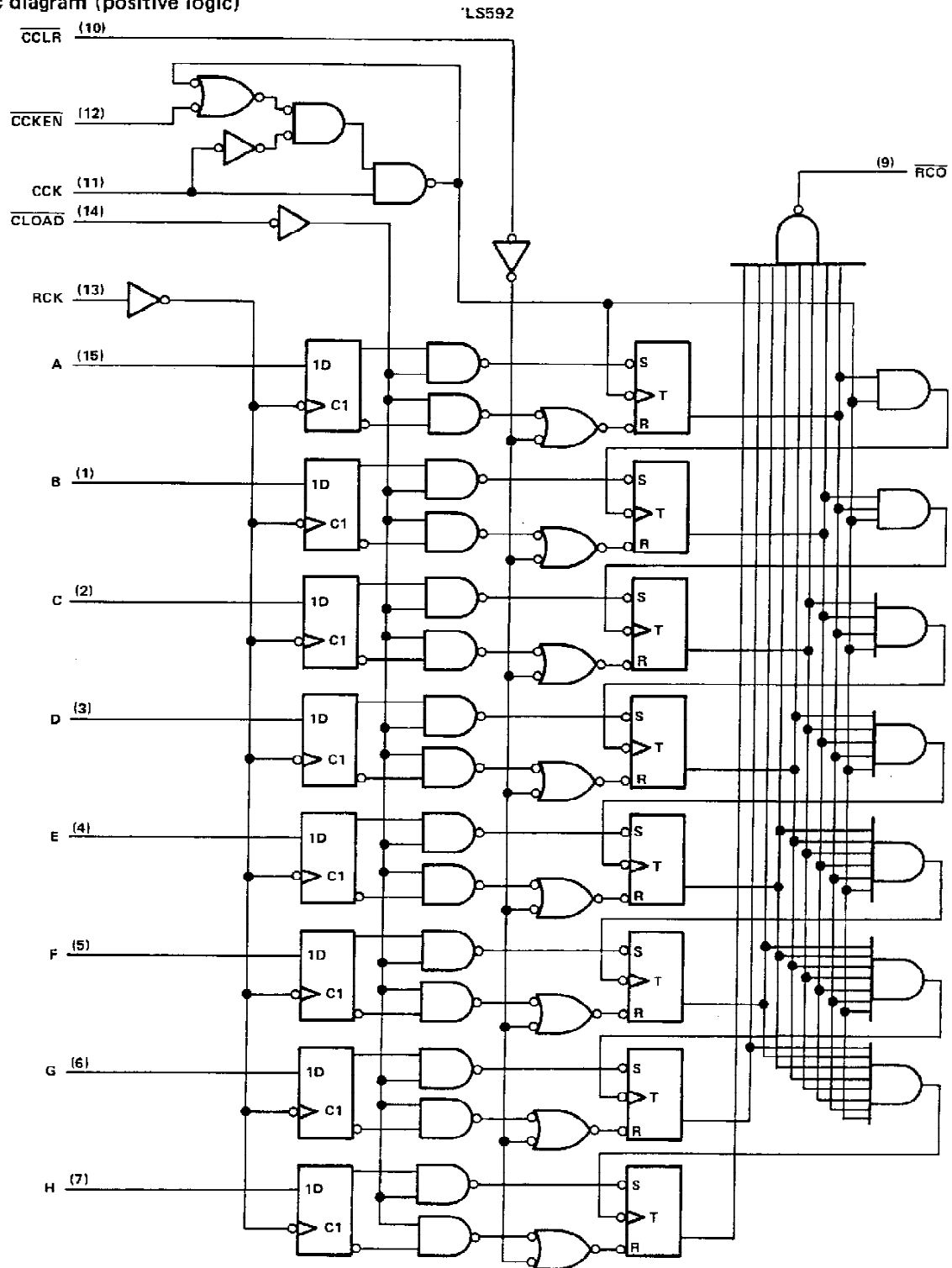
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

SN54LS592, SN74LS592 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic diagram (positive logic)

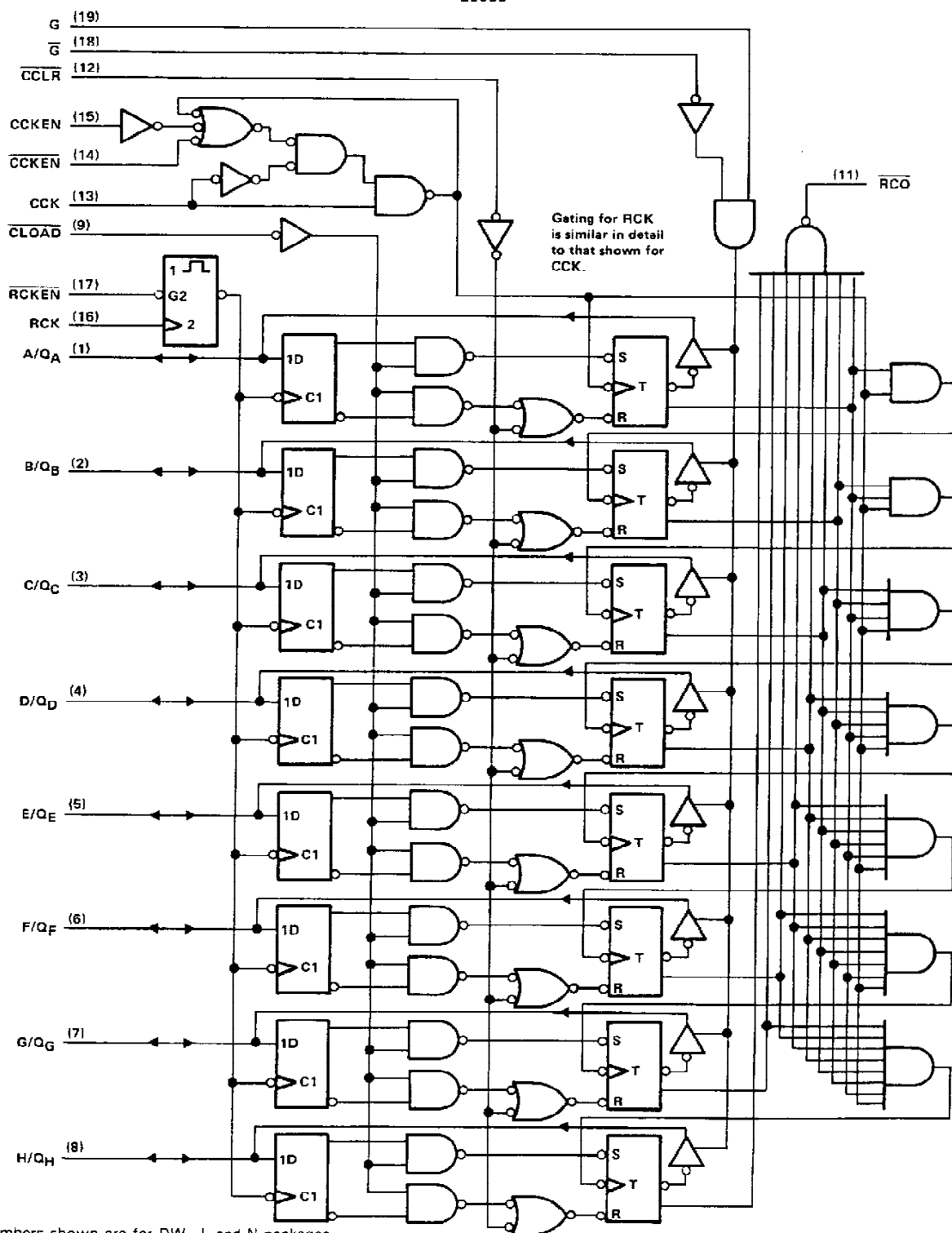


Pin numbers shown are for J, N, and W packages.

SN54LS593, SN74LS593 **8-BIT BINARY COUNTERS WITH INPUT REGISTERS**

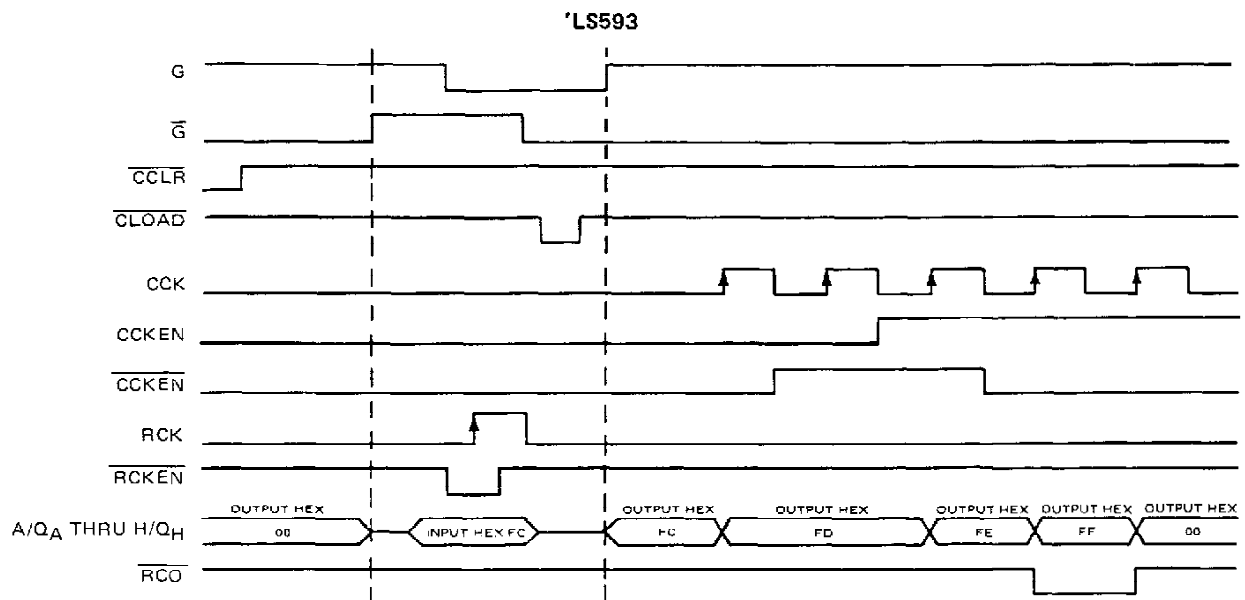
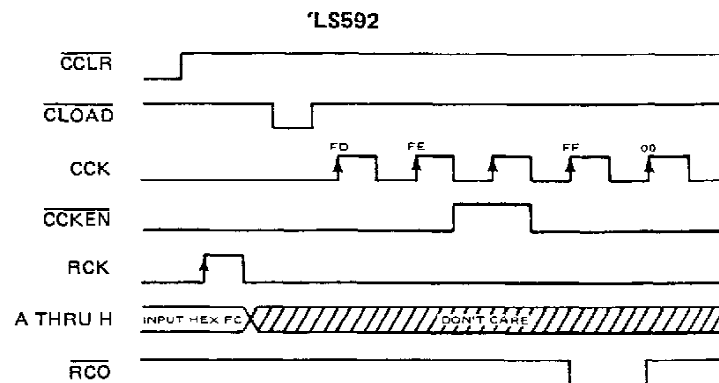
logic diagram (positive logic)

'LS593



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8-BIT BINARY COUNTERS WITH INPUT REGISTERS

typical operating sequences



SN54LS592, SN54LS593, SN74LS592, SN74LS593 **8-BIT BINARY COUNTERS WITH INPUT REGISTERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (excluding I/O ports)	7 V
Off-state output voltage (including I/O ports)	5.5 V
Operating free-air temperature range: SN54LS592, SN54LS593	– 55°C to 125°C
SN74LS592, SN74LS593	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current	\overline{RCO}		– 1			– 1	mA
		Q 'LS593 only		– 1			– 2.6	
I_{OL}	Low-level output current	\overline{RCO}		8			16	mA
		Q 'LS593 only		12			24	
f_{CCK}	Counter clock frequency	0		20	0		20	MHz
$t_w (CCK)$	Duration of counter clock pulse	25			25			ns
$t_w (CCLR)$	Duration of counter clear pulse	20			20			ns
$t_w (RCK)$	Duration of register clock pulse	20			20			ns
$t_w (CLOAD)$	Duration of counter load pulse	40			40			ns
t_{su}	Register enable setup time	\overline{RCKEN} low to $\overline{RCK} \uparrow$, 'LS593		20			20	ns
t_{su}	Counter enable setup time before $\overline{CCK} \uparrow$	\overline{CCKEN} low, 'LS592		30			30	ns
		\overline{CCKEN} low or						
		\overline{CCKEN} high, 'LS593		30			30	
t_{su}	Setup time	\overline{CCLR} inactive before $\overline{CCK} \uparrow$		20			20	ns
		\overline{CLOAD} inactive before $\overline{CCK} \uparrow$		20			20	
		$\overline{RCK} \uparrow$ before $\overline{CLOAD} \uparrow$ (see Note 2)		30			30	
		Data A thru H before $\overline{RCK} \uparrow$		20			20	
t_h	Hold time	Data A thru H after $\overline{RCK} \uparrow$		0			0	ns
		All others		0			0	
T_A	Operating free-air temperature	– 55		125	0		70	°C

NOTE 2: This time insures the data saved by $\overline{RCK} \uparrow$ will also be loaded into the counter.



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8-BIT BINARY COUNTERS WITH INPUT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS*		SN74LS*		UNIT
						MIN	TYP‡	MAX	MIN	
V _{IK}			V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5		V
V _{OH}	'LS593 Q		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -1 mA		2.4 3.2				V
				I _{OH} = -2.6 mA		2.4 3.1				
	RCO			I _{OH} = -1 mA		2.4 3.2		2.4 3.2		
V _{OL}	'LS593 Q		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA		0.25 0.4		0.25 0.4		V
				I _{OL} = 24 mA				0.35 0.5		
				I _{OL} = 8 mA		0.25 0.4		0.25 0.4		
	RCO			I _{OL} = 16 mA				0.35 0.5		
I _{OZH}	'LS593 Q		V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V, V _{IL} = MAX,			20		20		μA
I _{OZL}	'LS593 Q		V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V, V _{IL} = MAX,			-0.4		-0.4		mA
I _I	'LS593 Q		V _{CC} = MAX	V _I = 5.5 V		0.1		0.1		mA
	Others			V _I = 7 V		0.1		0.1		
I _{IH}			V _{CC} = MAX, V _I = 2.7 V			20		20		μA
I _{IL}	CCK		V _{CC} = MAX, V _I = 0.4 V			-0.8		-0.8		mA
	RCK	'LS592				-0.2		-0.2		
		'LS593				-0.8		-0.8		
	A thru H					-0.4		-0.4		
	Others					-0.2		-0.2		
I _{OS} §	'LS593 Q		V _{CC} = MAX, V _O = 0 V			-30 -130		-30 -130		mA
	RCO					-20 -100		-20 -100		
I _{CC}	'LS592	I _{CCH}	V _{CC} = MAX, All possible inputs grounded, All outputs open			40 60		40 60		mA
		I _{CCL}				40 60		40 60		
	'LS593	I _{CCH}				47 70		47 70		
		I _{CCL}				53 80		53 80		
		I _{CCZ}				57 85		57 85		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

TEXAS
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LS592			LS593			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CCK	\overline{RCO}	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	20	35		20	35		MHz
t_{PLH}	CCK \uparrow	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$				14	21		ns
t_{PHL}	CCK \downarrow	Q					26	39		ns
t_{PLH}	\overline{CLOAD} \downarrow	Q					34	51		ns
t_{PHL}	\overline{CLOAD} \uparrow	Q					28	42		ns
t_{PHL}	\overline{CCLR} \downarrow	Q					25	38		ns
t_{PZH}	G \uparrow	Q					31	47		ns
t_{PZL}	G \uparrow	Q					27	40		ns
t_{PZH}	\overline{G} \downarrow	Q					29	45		ns
t_{PZL}	\overline{G} \downarrow	Q					31	47		ns
t_{PHZ}	G \downarrow	Q					33	50		ns
t_{PLZ}	G \downarrow	Q	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$				35	52		ns
t_{PHZ}	\overline{G} \uparrow	Q					26	39		ns
t_{PLZ}	\overline{G} \uparrow	Q					28	42		ns
t_{PLH}	CCK \uparrow	\overline{RCO}								
t_{PHL}	CCK \downarrow	\overline{RCO}	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	15	23		14	21		ns
t_{PLH}	\overline{CLOAD} \downarrow	\overline{RCO}		20	30		20	30		ns
t_{PHL}	\overline{CLOAD} \uparrow	\overline{RCO}		31	47		31	47		ns
t_{PLH}	\overline{CCLR} \downarrow	\overline{RCO}		27	41		27	41		ns
t_{PHL}	\overline{CCLR} \uparrow	\overline{RCO}		30	45		30	45		ns
t_{PLH}	RCK \uparrow	\overline{RCO}	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	35	53		42	63		ns
t_{PHL}	RCK \downarrow	\overline{RCO}	$\overline{CLOAD} = L$	30	45		33	50		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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