

SN74LS222A, SN74LS224A 16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES WITH 3-STATE OUTPUTS

SDLS023 – JANUARY 1991 – REVISED SEPTEMBER 1993

- Independent Synchronous Inputs and Outputs
- 16 Words by 4 Bits Each
- 3-State Outputs Drive Bus Lines Directly
- Data Rates From 0 to 10 MHz
- Fall-Through Time . . . 50 ns Typ
- Data Terminals Arranged for Printed-Circuit-Board Layout
- Expandable Using External Gating
- Packaged in Standard Plastic 300-mil DIPs

description

These 64-bit memories are low-power Schottky memory arrays organized as 16 words by 4 bits each. They can be expanded in multiples of $15m + 1$ words or $4n$ bits or both (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array). However, some external gating is required (see Figure 1). For longer words using the SN74LS224A, the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization.

An input-ready enable (IRE) and output-ready enable (ORE) are included in the SN74LS222A only.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 10 MHz in a bit-parallel format, word by word.

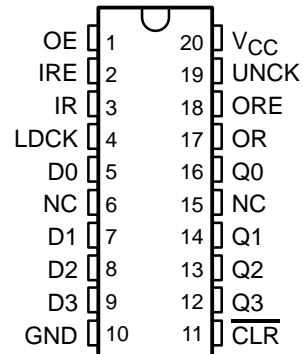
Data is written into memory on a low-to-high transition at the load-clock (LDCK) input and is read out on a low-to-high transition at the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the input-ready (IR) and output-ready (OR) flags that indicate not-full and not-empty conditions. IR is high only when the memory is not full and the LDCK is low. OR is high only when the memory is not empty and UNCK is high.

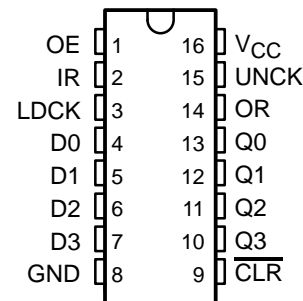
A low level on the clear ($\overline{\text{CLR}}$) input resets the internal stack-control pointers and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the IR and OR outputs.

The SN74LS222A and SN74LS224A are characterized for operation from 0°C to 70°C.

SN74LS222A . . . N PACKAGE
(TOP VIEW)



SN74LS224A . . . N PACKAGE
(TOP VIEW)



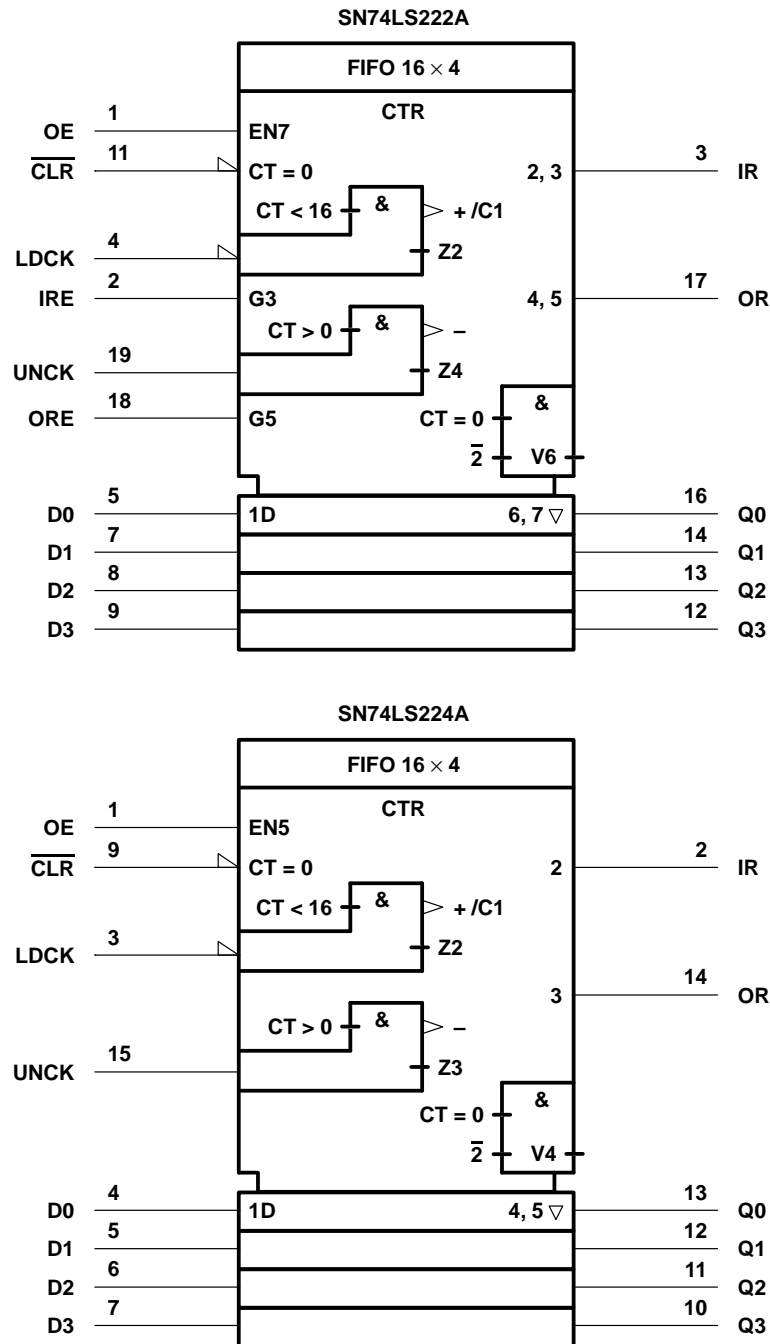
NC – No internal connection

SN74LS222A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES WITH 3-STATE OUTPUTS

SDLS023 – JANUARY 1991 – REVISED SEPTEMBER 1993

logic symbols†



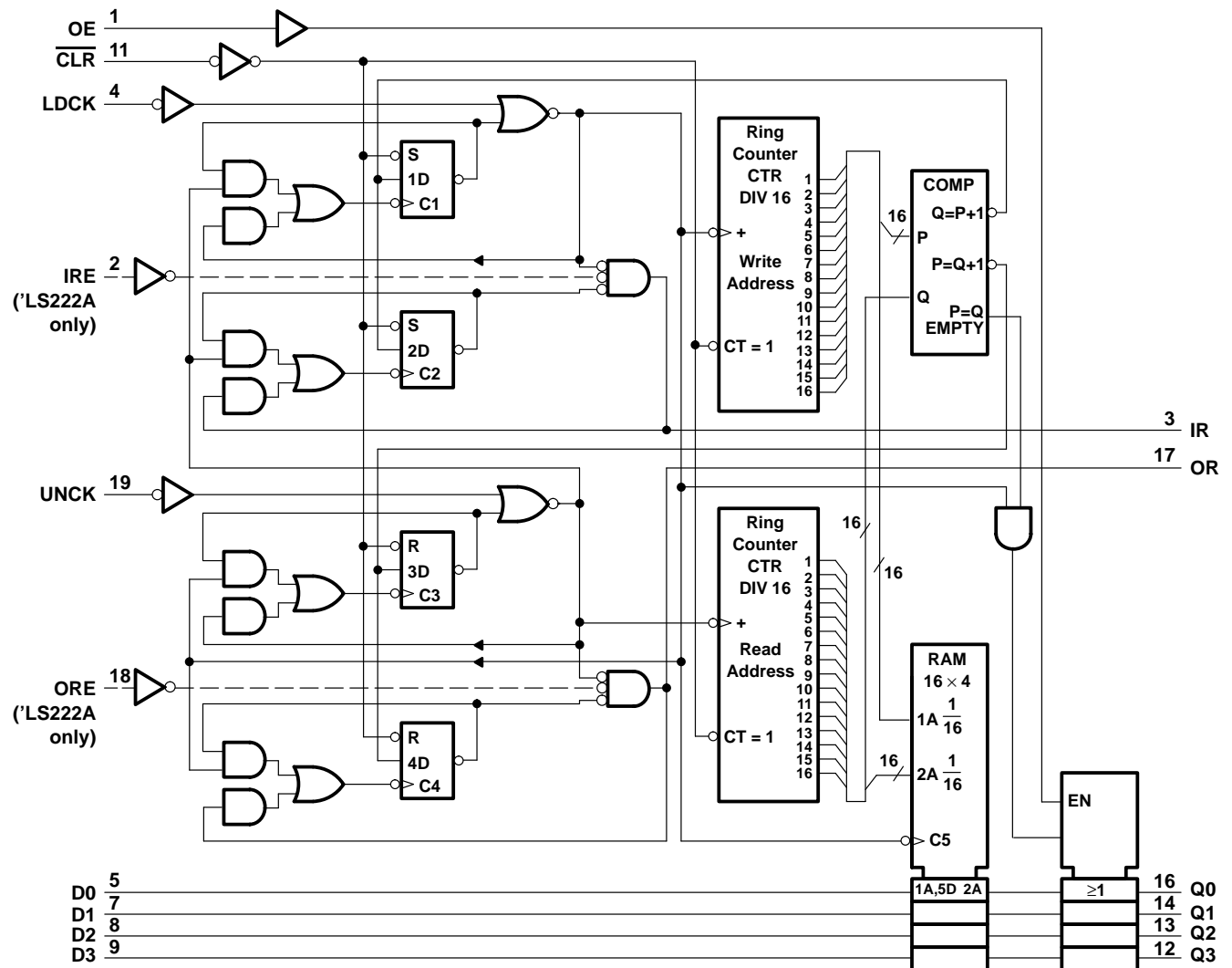
† These symbols are in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. These symbols are functionally accurate but do not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

SN74LS222A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES WITH 3-STATE OUTPUTS

SDLS023 – JANUARY 1991 – REVISED SEPTEMBER 1993

logic diagram (positive logic)



Pin numbers shown are for the 20-pin N package.

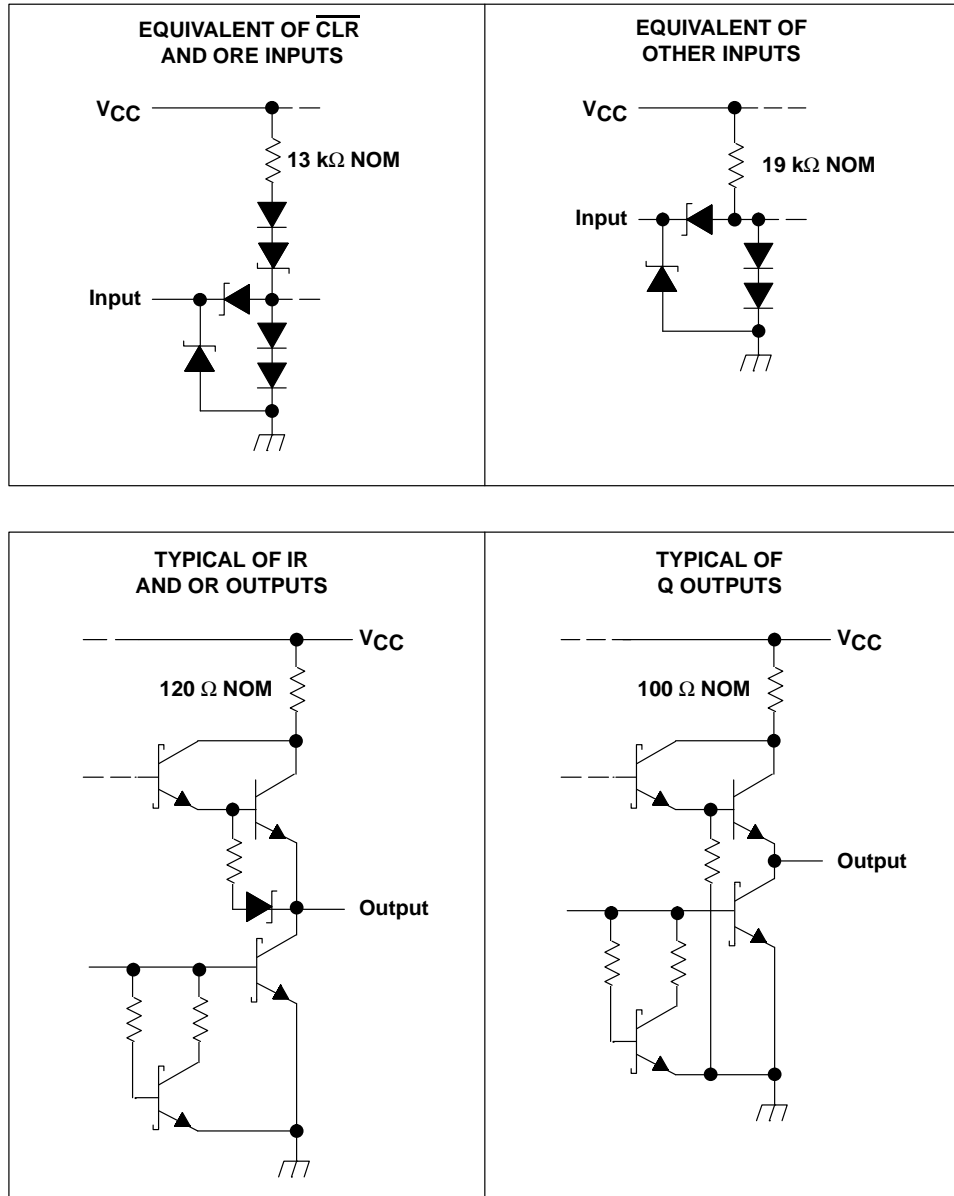
SN74LS222A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023 – JANUARY 1991 – REVISED SEPTEMBER 1993

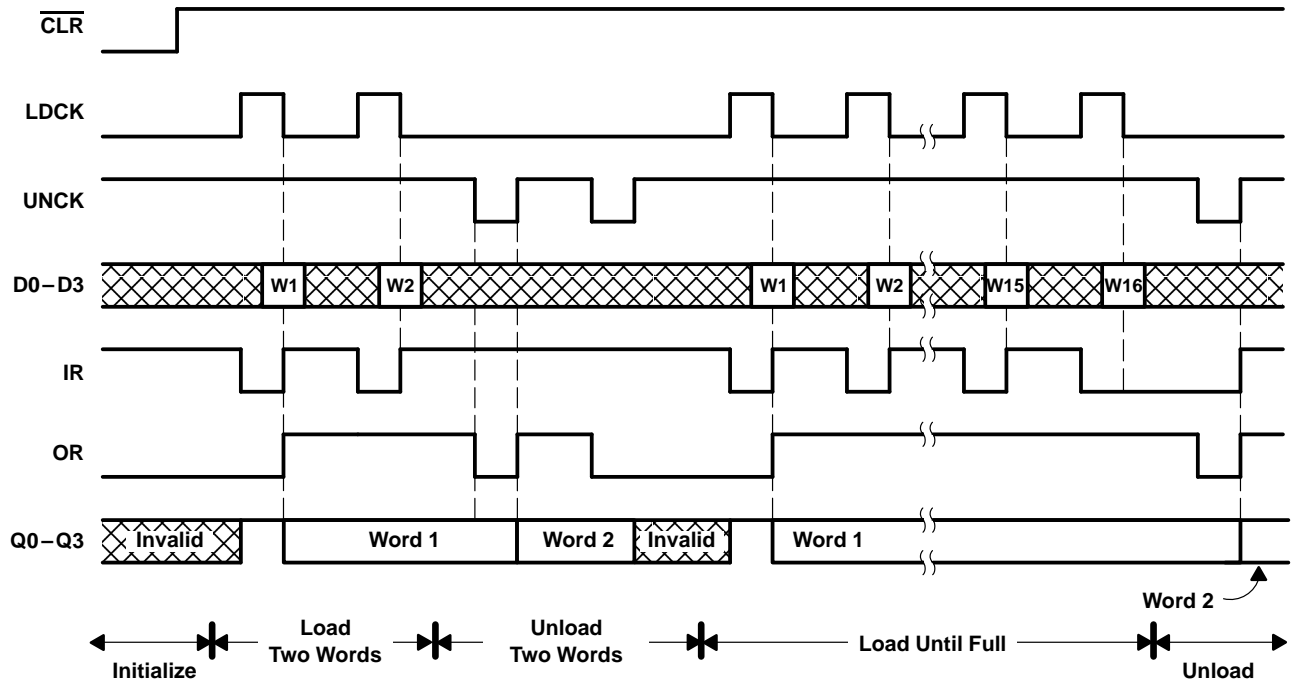
schematics of inputs and outputs



SN74LS222A, SN74LS224A
16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES
WITH 3-STATE OUTPUTS

SDLS023 – JANUARY 1991 – REVISED SEPTEMBER 1993

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Off-state output voltage, V_O	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

SN74LS222A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023 – JANUARY 1991 – REVISED SEPTEMBER 1993

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current	Q outputs		–2.6	mA
		IR, OR		–0.4	
I _{OL}	Low-level output current	Q outputs		24	mA
		IR, OR		8	
t _w	Pulse duration	LDCK high		60	ns
		LDCK low		15	
		UNCK low		30	
		UNCK high		30	
		CLR low		20	
t _{su}	Setup time	Data to LDCK↓		50	ns
		LDCK↓ before UNCK↓		50	
		UNCK↑ before LDCK↑		50	
t _h	Hold time	Data from LDCK↓		10	ns
T _A	Operating free-air temperature	0		70	°C

NOTE 2: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.75 V,	I _I = –18 mA			–1.5	V
V _{OH}	Q outputs	V _{CC} = 4.75 V,	I _{OH} = –2.6 mA	2.4	3.4		V
	IR, OR	V _{CC} = 4.75 V,	I _{OH} = –0.4 mA	2.7	3.4		
V _{OL}	Q outputs	V _{CC} = 4.75 V	I _{OL} = 12 mA		0.25	0.4	V
			I _{OL} = 24 mA		0.35	0.5	
	IR, OR	V _{CC} = 4.75 V	I _{OL} = 4 mA		0.25	0.4	
			I _{OL} = 8 mA		0.35	0.5	
I _{OZH}	Q outputs	V _{CC} = 5.25 V,	V _O = 2.7 V			20	μA
I _{OZL}	Q outputs	V _{CC} = 5.25 V,	V _O = 0.4 V			–20	μA
I _I		V _{CC} = 5.25 V,	V _I = 7 V			0.1	mA
I _{IH}		V _{CC} = 5.25 V,	V _I = 2.7 V			20	μA
I _{IL}		V _{CC} = 5.25 V,	V _I = 0.4 V			–0.4	mA
I _{OS‡}	Q outputs	V _{CC} = 5.25 V		–30		–130	mA
	IR, OR			–20		–100	
I _{CC}		V _{CC} = 5.25 V	Outputs high		84	135	mA
			Outputs low		87	155	
			Outputs disabled		89	155	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.



SN74LS222A, SN74LS224A
16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES
WITH 3-STATE OUTPUTS

SDLS023 – JANUARY 1991 – REVISED SEPTEMBER 1993

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN74LS222A		SN74LS224A		UNIT
				TYP	MAX	TYP	MAX	
tPLH	IRE↑	IR	R _L = 2 kΩ, C _L = 15 pF	23	35	N/A	N/A	ns
tPHL	IRE↓			9	15	N/A	N/A	
tPLH	ORE↑	OR		22	35	N/A	N/A	ns
tPHL	ORE↓			9	15	N/A	N/A	
tPLH	LDCK↓	IR		25	40	25	40	ns
tPHL	LDCK↑			36	50	36	50	
tPLH	LDCK↓	OR		48	70	48	70	ns
tPLH	UNCK↑	OR		29	45	29	45	ns
tPHL	UNCK↓			28	45	28	45	
tPLH	UNCK↑	IR		49	70	49	70	ns
tPLH	CLR↓	IR		36	55	36	55	ns
tPHL		OR		25	40	25	40	
tPHL	LDCK↓	Q	R _L = 667 Ω, C _L = 45 pF	34	50	34	50	ns
tPLH	UNCK↑	Q		54	80	54	80	ns
tPHL				45	70	45	70	
tPZL	OE↑	Q		22	35	22	35	ns
tPZH				21	35	21	35	
tPLZ	OE↓	Q	R _L = 667 Ω, C _L = 5 pF	16	30	16	30	ns
tPHZ				18	30	18	30	

NOTE 3: Load circuit and voltage waveforms are shown in Section 1 of the 1988 *TTL Logic Data Book*, literature #SDLD001A.

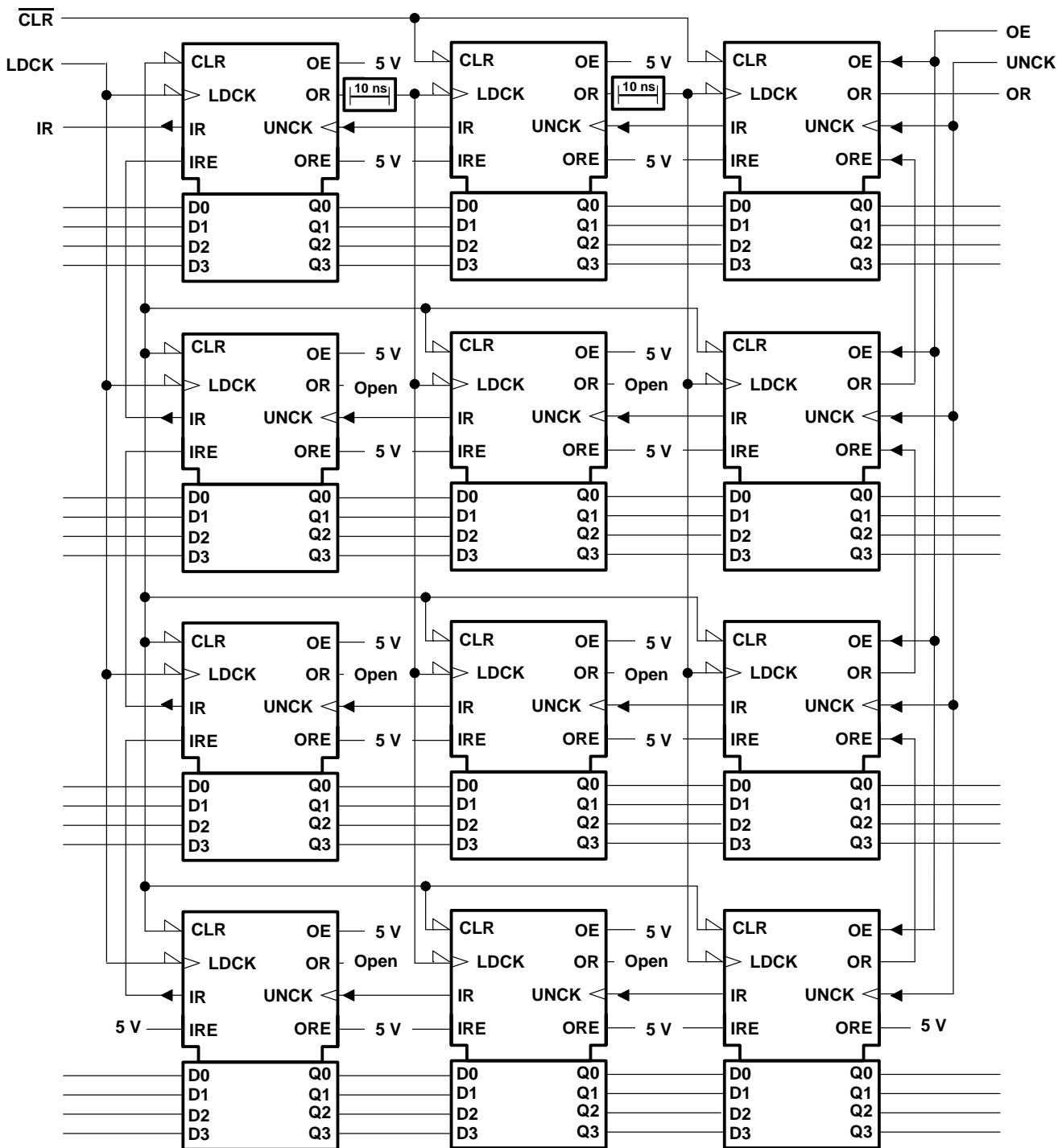
SN74LS222A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023 – JANUARY 1991 – REVISED SEPTEMBER 1993

APPLICATION INFORMATION



10 ns = Noninverting delay ≥ 10 ns (e.g., two stages of 'LS04), two places.

Figure 1. 48-Word by 16-Bit Expansion Using 'LS222A

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.