

# SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

SDLS063

OCTOBER 1976 - REVISED MARCH 1988

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'166	35 MHz	360 mW
'LS166A	35 MHz	100 mW

## description

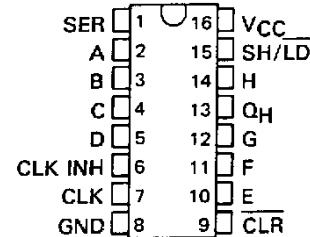
The '166 and 'LS166A 8-bit shift registers are compatible with most other TTL logic families. All '166 and 'LS166A inputs are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

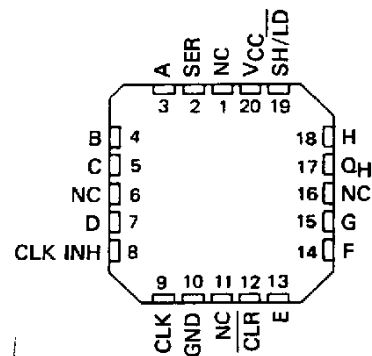
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>H</sub>
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	L	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	X	H	↑	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>

SN54166, SN54LS166A . . . J OR W PACKAGE  
SN74166 . . . N PACKAGE  
SN74LS166A . . . D OR N PACKAGE  
(TOP VIEW)

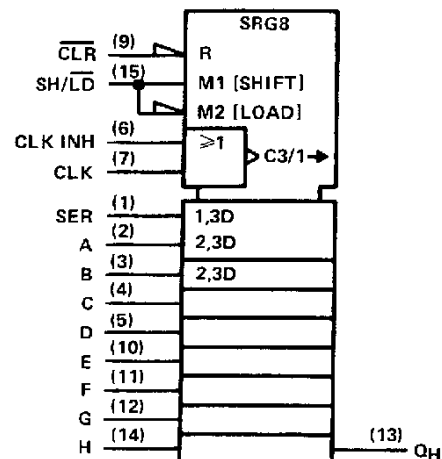


SN54LS166A . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

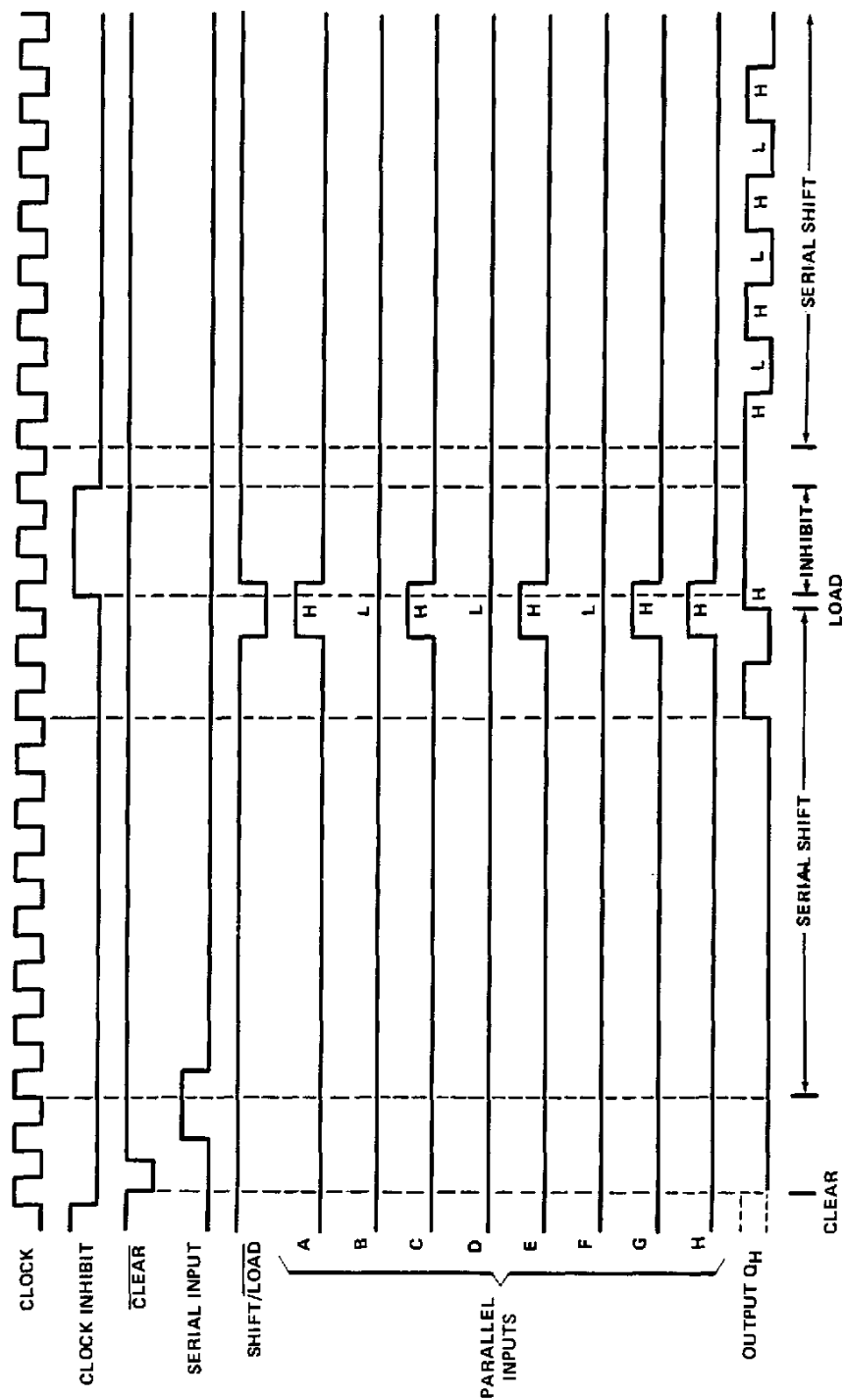
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**PARALLEL-LOAD 8-BIT SHIFT REGISTERS**

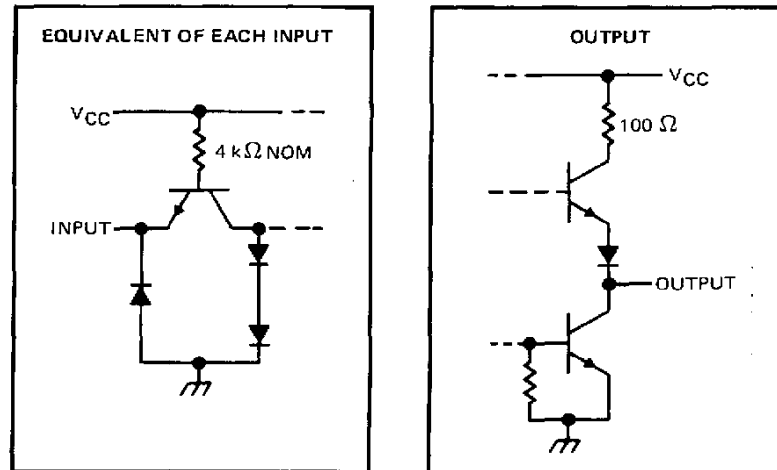
typical clear, shift, load, inhibit, and shift sequences



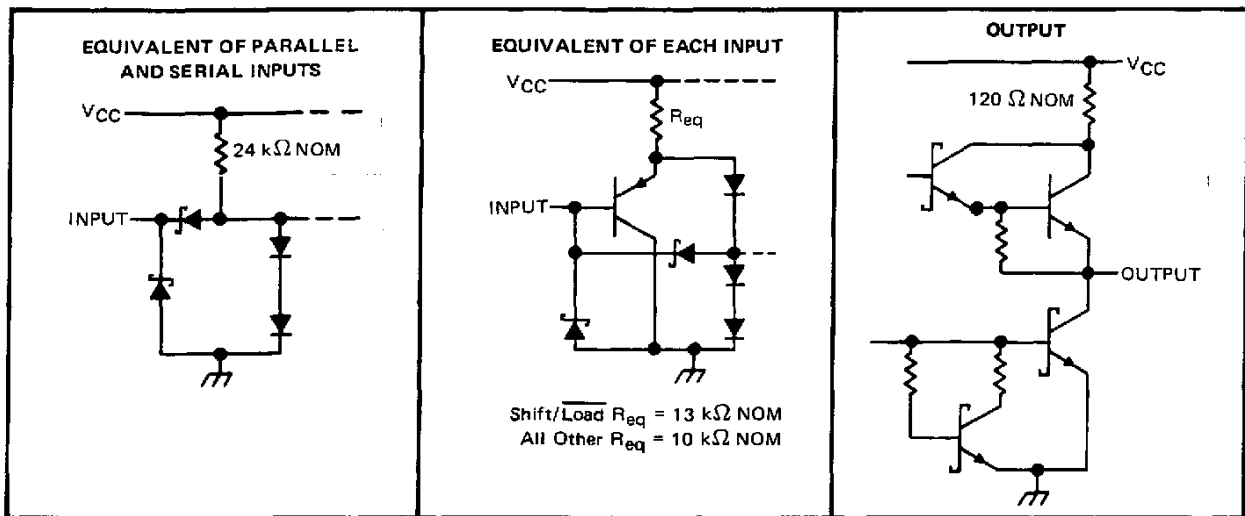
**SN54166, SN54LS166A, SN74166, SN74LS166A**  
**PARALLEL-LOAD 8-BIT SHIFT REGISTERS**

schematics of inputs and outputs

'166



'LS166A



**logic diagram (positive logic)**



# SN54166, SN74166 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54166 (see Note 2)	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74166	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

recommended operating conditions

	SN54166			SN74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu\text{A}$
Low-level output current, $I_{OL}$			16			16	mA
Clock frequency, $f_{\text{clock}}$	0		25	0		25	MHz
Width of clock or clear pulse, $t_W$ (see Figure 1)	20			20			ns
Mode-control setup time, $t_{SU}$	30			30			ns
Data setup time, $t_{SD}$ (see Figure 1)	20			20			ns
Hold time at any input, $t_H$ (see Figure 1)	0			0			ns
Operating free-air temperature, $T_A$ (see Note 2)	-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54166			SN74166			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.8			0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}$ Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		90	127		90	127	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. An SN54166 in the W package operating at free-air temperatures above  $113^{\circ}\text{C}$  requires a heat-sink that provides a thermal resistance from case to free air,  $R_{\theta CA}$ , of not more than  $48^{\circ}\text{C/W}$ .

3. With all outputs open, 4.5 V applied to the serial input, all other inputs except the clock grounded,  $I_{CC}$  is measured after a momentary ground, then 4.5 V, is applied to the clock.

switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{max}}$ Maximum clock frequency		25	35		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear			23	35	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Figure 1		20	30	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock			17	26	ns

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# SN54LS166A, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS166A	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74LS166A	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54LS166A			SN74LS166A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{\text{clock}}$	Clock frequency	0		25	0		25	MHz
$t_w$	Width of clear pulse (See Figure 1)	20			20			ns
$t_w$	Width of clock pulse (See Figure 1)	25			25			
$t_{su}$	Mode-control setup time	30			30			ns
$t_{su}$	Data setup time (See Figure 1)	20			20			ns
$t_h$	Hold time at any input (See Figure 1 and Note 4)	0			0			ns
$T_A$	Operating free air temperature	-55		125	0		70	$^{\circ}\text{C}$

NOTE 4: The hold time limit of 0 ns applies only if the rise time is less than or equal to 10 ns.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS166A		SN74LS166A		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = - 18 mA			- 1.5		- 1.5	V	
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = - 0.4 mA	2.5	3.4		2.7	3.4	V	
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 4 mA		0.25	0.4	0.25	0.4	V
		I <sub>OL</sub> = 8 mA				0.35	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1		0.1	mA	
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20		20	μA	
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			- 0.4		- 0.4	mA	
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	- 20		- 100	- 20	- 100	mA	
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 5	20	32		20	32	mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§Not more than one output should be shorted at a time, and duration for short-circuit should not exceed one second.

NOTE 5: With all outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded,  $I_{CC}$  is measured after a momentary ground, than 4.5 V, is applied to clock.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

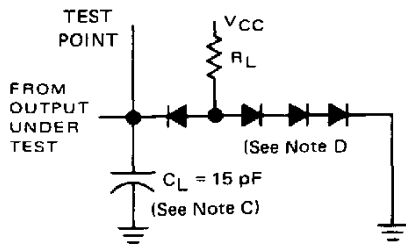
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{max}}$ Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Figure 1	25	35		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear			19	30	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock		7	14	25	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock		5	11	20	ns

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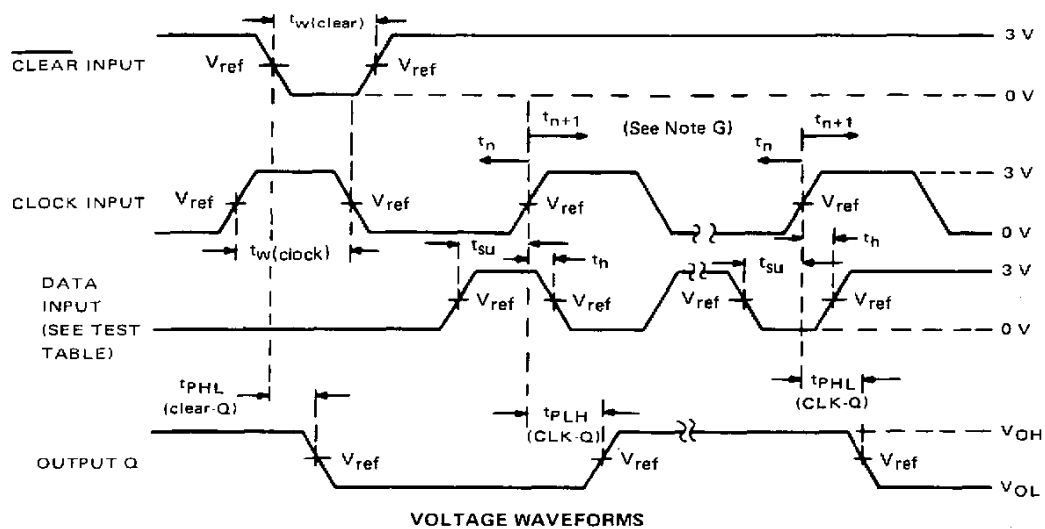
## PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE F)
H	0 V	$Q_H$ at $t_{n+1}$
Serial Input	4.5 V	$Q_H$ at $t_{n+8}$



VOLTAGE WAVEFORMS

- NOTE: A. All pulse generators have the following characteristics:  $Z_{out} = 50\Omega$ ; for '166,  $t_r \leq 7$  ns and  $t_f \leq 7$  ns; for 'LS166A,  $t_r \leq 15$  ns and  $t_f \leq 6$  ns.
- B. The clock pulse has the following characteristics:  $t_w(\text{clock}) \leq 20$  ns and  $\text{PRR} = 1$  MHz. The clear pulse has the following characteristics:  $t_w(\text{clear}) \leq 20$  ns and  $t_{hold} = 0$  ns. When testing  $f_{max}$ , vary the clock PRR.
- C.  $C_L$  includes probe and jig capacitance.
- D. All diodes are 1N3064, 1N916, or equivalent.
- E. A clear pulse is applied prior to each test.
- F. Propagation delay times ( $t_{pLH}$  and  $t_{pHL}$ ) are measured at  $t_{n+1}$ . Proper shifting of data is verified at  $t_{n+8}$  with a functional test.
- G.  $t_n$  = bit time before clocking transition  
 $t_{n+1}$  = bit time after one clocking transition  
 $t_{n+8}$  = bit time after eight clocking transitions
- H. For '166  $V_{ref} = 1.5$  V; for 'LS166A  $V_{ref} = 1.3$  V.

FIGURE 1