

# SN54259, SN54LS259B, SN74259, SN74LS259B 8-BIT ADDRESSABLE LATCHES

SDLS086

DECEMBER 1983 — REVISED MARCH 1988

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplified Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

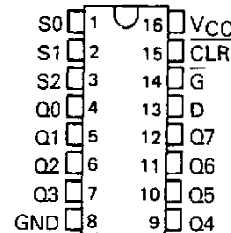
These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear (CLR) and enable (G) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable G should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54259 and SN54LS259B are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74259 and SN74LS259B are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

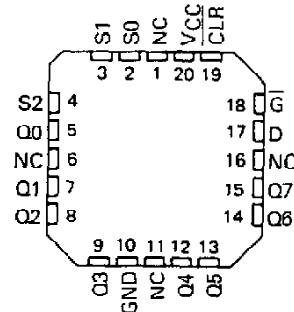
SN54259, SN54LS259B . . . J OR W PACKAGE  
SN74259 . . . N PACKAGE  
SN74LS259B . . . D OR N PACKAGE

(TOP VIEW)



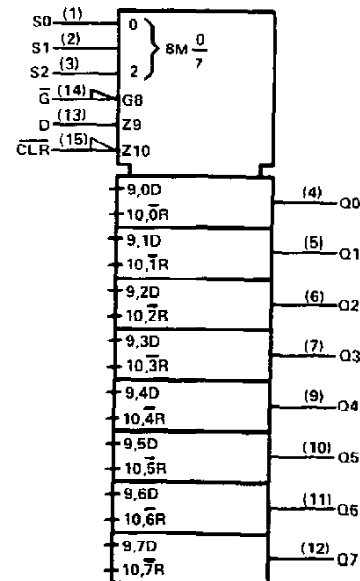
SN54LS259B . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

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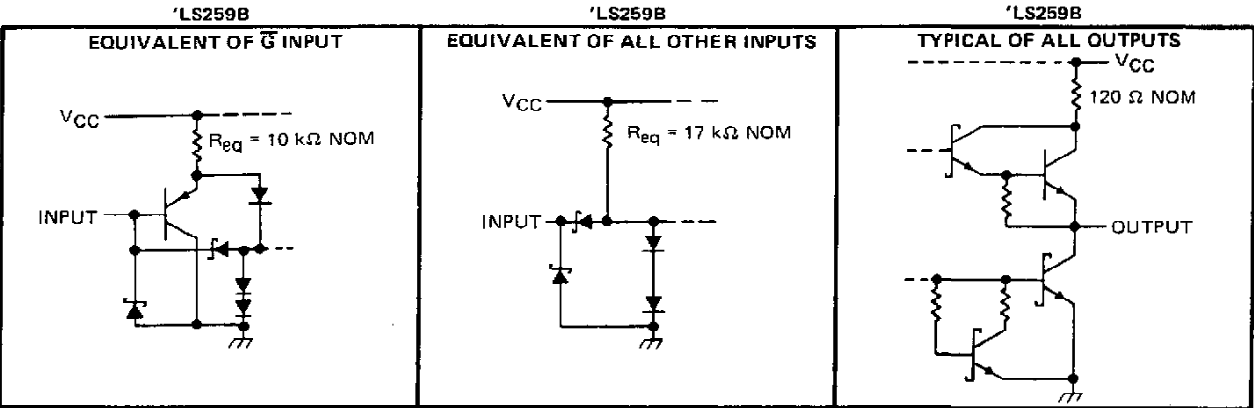
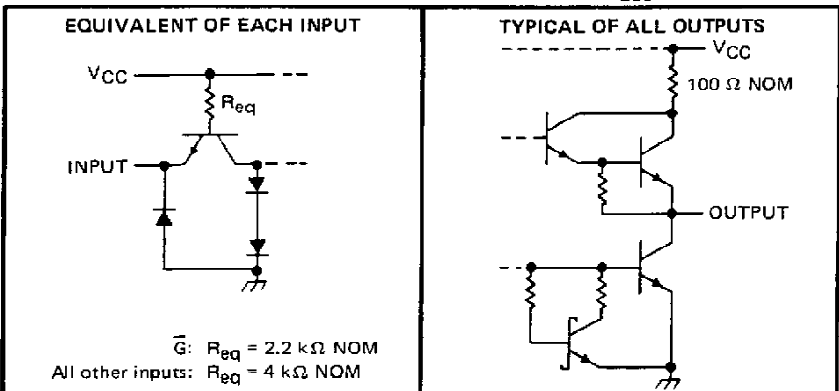
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| FUNCTION TABLE |   |                                 |                         | LATCH SELECTION TABLE |               |    |    |
|----------------|---|---------------------------------|-------------------------|-----------------------|---------------|----|----|
| INPUTS         |   | OUTPUT OF<br>ADDRESSED<br>LATCH | EACH<br>OTHER<br>OUTPUT | FUNCTION              | SELECT INPUTS |    |    |
| CLR            | G |                                 |                         |                       | S2            | S1 | S0 |
| H              | L | D                               | $Q_{i0}$                | Addressable Latch     | L             | L  | L  |
| H              | H | $Q_{i0}$                        | $Q_{i0}$                | Memory                | L             | L  | H  |
| L              | L | D                               | L                       | 8-Line Demultiplexer  | L             | H  | L  |
| L              | H | L                               | L                       | Clear                 | L             | H  | H  |
|                |   |                                 |                         |                       | H             | L  | L  |
|                |   |                                 |                         |                       | H             | L  | H  |
|                |   |                                 |                         |                       | H             | H  | L  |
|                |   |                                 |                         |                       | H             | H  | H  |

H = high level, L = low level  
D = the level at the data input  
 $Q_{i0}$  = the level of  $Q_i$  ( $i = 0, 1, \dots, 7$ , as appropriate) before the indicated steady-state input conditions were established.

schematic of inputs and outputs '259



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|   |                 |
|---|-----------------|
| Supply voltage (see Note 1)                               | 7 V             |
| Input voltage: SN54259, SN74259                           | 5.5 V           |
| SN54LS259B, SN74LS259B                                    | 7 V             |
| Operating free-air temperature range: SN54259, SN54LS259B | − 55°C to 125°C |
| SN74259, SN74LS259B                                       | 0°C to 70°C     |
| Storage temperature range                                 | − 65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.



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# SN54259, SN74259

## 8-BIT ADDRESSABLE LATCHES

### recommended operating conditions

|                                       |         | SN54259       |     |      | SN74259       |     |      | UNIT        |
|---------------------------------------|---------|---------------|-----|------|---------------|-----|------|-------------|
|                                       |         | MIN           | NOM | MAX  | MIN           | NOM | MAX  |             |
| Supply voltage, $V_{CC}$              |         | 4.5           | 5   | 5.5  | 4.75          | 5   | 5.25 | V           |
| High-level output current, $I_{OH}$   |         |               |     | -800 |               |     | -800 | $\mu A$     |
| Low-level output current, $I_{OL}$    |         |               |     | 16   |               |     | 16   | mA          |
| Width of clear or enable pulse, $t_W$ |         | 15            |     |      | 15            |     |      | ns          |
| Setup time, $t_{su}$                  | Data    | 15 $\uparrow$ |     |      | 15 $\uparrow$ |     |      | ns          |
|                                       | Address | 5 $\uparrow$  |     |      | 5 $\uparrow$  |     |      |             |
| Hold time, $t_h$                      | Data    | 0 $\uparrow$  |     |      | 0 $\uparrow$  |     |      | ns          |
|                                       | Address | 20 $\uparrow$ |     |      | 20 $\uparrow$ |     |      |             |
| Operating free-air temperature, $T_A$ |         | -55           |     | 125  | 0             |     | 70   | $^{\circ}C$ |

$\uparrow$ The arrow indicates that the rising edge of the enable pulse is used for reference.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS $^{\dagger}$  | SN54259 |                |      | SN74259 |                |      | UNIT    |
|-----------|--|---|---------|----------------|------|---------|----------------|------|---------|
|           |  |   | MIN     | TYP $\ddagger$ | MAX  | MIN     | TYP $\ddagger$ | MAX  |         |
| $V_{IH}$  | High-level input voltage               |   | 2       |                |      | 2       |                |      | V       |
| $V_{IL}$  | Low-level input voltage                |   |         |                | 0.8  |         |                | 0.8  | V       |
| $V_{IK}$  | Input clamp voltage                    | $V_{CC} = \text{MIN}, I_I = 12 \text{ mA}$  |         |                | -1.5 |         |                | -1.5 | V       |
| $V_{OH}$  | High-level output voltage              | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu A$    | 2.4     | 3.4            |      | 2.4     | 3.4            |      | V       |
| $V_{OL}$  | Low-level output voltage               | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$ |         | 0.2            | 0.4  |         | 0.2            | 0.4  | V       |
| $I_I$     | Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$  |         |                | 1    |         |                | 1    | mA      |
| $I_{IH}$  | High-level input current               | $\bar{G}$   |         |                | 80   |         |                | 80   | $\mu A$ |
|           |  | Other inputs  |         |                | 40   |         |                | 40   |         |
| $I_{IL}$  | Low-level input current                | $\bar{G}$   |         |                | -3.2 |         |                | -3.2 | mA      |
|           |  | Other inputs  |         |                | -1.6 |         |                | -1.6 |         |
| $I_{OS}$  | Short-circuit output current $^{\S}$   | $V_{CC} = \text{MAX}$   | -18     |                | -57  | -18     |                | -57  | mA      |
| $I_{CC}$  | Supply current                         | $V_{CC} = \text{MAX},$ See Note 2   |         | 60             | 90   |         | 60             | 90   | mA      |

$^{\dagger}$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

$^{\ddagger}$ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$ .

$^{\S}$ Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with the inputs grounded and the outputs open.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|--|-----|-----|-----|------|
| t <sub>PHL</sub> | CLR             | Any Q          | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 400 Ω,<br>See Note 3 |     | 16  | 25  | ns   |
| t <sub>PLH</sub> | Data            | Any Q          |  |     | 14  | 24  | ns   |
| t <sub>PHL</sub> |                 |                |  |     | 11  | 20  |      |
| t <sub>PLH</sub> | Address         | Any Q          |  |     | 15  | 28  | ns   |
| t <sub>PHL</sub> |                 |                |  |     | 17  | 28  |      |
| t <sub>PLH</sub> | G               | Any Q          |  |     | 12  | 20  | ns   |
| t <sub>PHL</sub> |                 |                |  |     | 11  | 20  |      |

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

# SN54LS259B, SN74LS259B

## 8-BIT ADDRESSABLE LATCHES

### recommended operating conditions

|                 |                                |  | SN54LS259B |     |     | SN74LS259B |     |      | UNIT |
|-----------------|--------------------------------|--|------------|-----|-----|------------|-----|------|------|
|                 |                                |  | MIN        | NOM | MAX | MIN        | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                 |  | 4.5        | 5   | 5.5 | 4.75       | 5   | 5.25 | V    |
| V <sub>IH</sub> | High-level input voltage       |  | 2          |     |     | 2          |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage        |  | 0.7        |     |     | 0.8        |     |      | V    |
| I <sub>OH</sub> | High-level output current      |  | − 0.4      |     |     | − 0.4      |     |      | mA   |
| I <sub>OL</sub> | Low-level output current       |  | 4          |     |     | 8          |     |      | mA   |
| t <sub>W</sub>  | Pulse duration                 | $\overline{G}$ low                       | 17         |     |     | 17         |     |      | ns   |
|                 |                                | CLR low                                  | 10         |     |     | 10         |     |      |      |
| t <sub>SU</sub> | Set up time                    | Data before $\overline{G} \uparrow$      | 20         |     |     | 20         |     |      | ns   |
|                 |                                | Address before $\overline{G} \uparrow$   | 17         |     |     | 17         |     |      |      |
|                 |                                | Address before $\overline{G} \downarrow$ | 0          |     |     | 0          |     |      |      |
| t <sub>H</sub>  | Hold time                      | Data after $\overline{G} \uparrow$       | 0          |     |     | 0          |     |      | ns   |
|                 |                                | Address after $\overline{G} \uparrow$    | 0          |     |     | 0          |     |      |      |
| T <sub>A</sub>  | Operating free-air temperature |  | − 55       |     |     | 125        |     |      | °C   |
|                 |                                |  | − 55       |     |     | 125        |     |      | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS†  |                         | SN54LS259B |      |      | SN74LS259B |      |      | UNIT |
|-----------|---|-------------------------|------------|------|------|------------|------|------|------|
|           |   |                         | MIN        | TYP  | MAX  | MIN        | TYP  | MAX  |      |
| $V_{IK}$  | $V_{CC} = \text{MIN.}$ , $I_I = -18 \text{ mA}$   |                         |            |      | -1.5 |            |      | -1.5 | V    |
| $V_{OH}$  | $V_{CC} = \text{MIN.}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX.}$ , $I_{OH} = -0.4 \text{ mA}$ |                         | 2.5        | 3.4  |      | 2.7        | 3.4  |      | V    |
| $V_{OL}$  | $V_{CC} = \text{MIN.}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX.}$                              | $I_{OL} = 4 \text{ mA}$ | 0.25       | 0.4  |      | 0.25       | 0.4  |      | V    |
|           |   | $I_{OL} = 8 \text{ mA}$ |            |      |      | 0.35       | 0.5  |      |      |
| $I_I$     | $V_{CC} = \text{MAX.}$ , $V_I = 7 \text{ V}$  |                         |            | 0.1  |      |            | 0.1  |      | mA   |
| $I_{IH}$  | $V_{CC} = \text{MAX.}$ , $V_I = 2.7 \text{ V}$  |                         |            | 20   |      |            | 20   |      | μA   |
| $I_{IL}$  | $V_{CC} = \text{MAX.}$ , $V_I = 0.4 \text{ V}$  |                         |            | -0.4 |      |            | -0.4 |      | mA   |
| $I_{OS§}$ | $V_{CC} = \text{MAX.}$  |                         | -20        | -100 |      | -20        | -100 |      | mA   |
| $I_{CC}$  | $V_{CC} = \text{MAX.}$ , See Note 2   |                         | 27         | 36   |      | 22         | 36   |      | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ .

§ Not more than one output should be shorted at a time, and duration short-circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with the inputs grounded and the outputs open.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ \text{C}$

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|---|-----|-----|-----|------|
| t <sub>PHL</sub> | CLR             | Any Q          | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 2 kΩ,<br>See Note 3 | 12  | 18  |     | ns   |
| t <sub>PLH</sub> | Data            | Any Q          |   | 19  | 30  |     | ns   |
| t <sub>PHL</sub> |                 |                |   | 13  | 20  |     |      |
| t <sub>PLH</sub> | Address         | Any Q          |   | 17  | 27  |     | ns   |
| t <sub>PHL</sub> |                 |                |   | 14  | 20  |     |      |
| t <sub>PLH</sub> | $\overline{G}$  | Any Q          |   | 15  | 24  |     | ns   |
| t <sub>PHL</sub> |                 |                |   | 15  | 24  |     |      |

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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