

SDLS132

SN54LS137, SN74LS137 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

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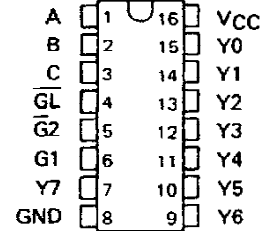
- Combines Decoder and 3-Bit Address Latch
- Incorporates 2 Enable Inputs to Simplify Cascading
- Low Power Dissipation . . . 65 mW Typ

description

The 'LS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input (\overline{GL}) is low, the 'LS137 acts as a decoder/demultiplexer. When \overline{GL} goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as \overline{GL} remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'LS137 is ideally suited for implementing glitch free decoders in strobed (stored-address) applications in bus-oriented systems.

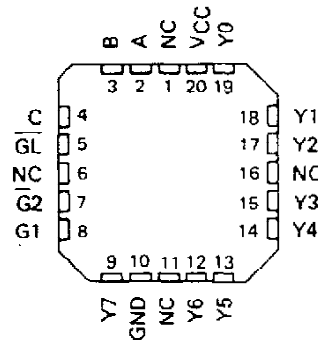
SN54LS137 . . . J OR W PACKAGE
SN74LS137 . . . D OR N PACKAGE

(TOP VIEW)



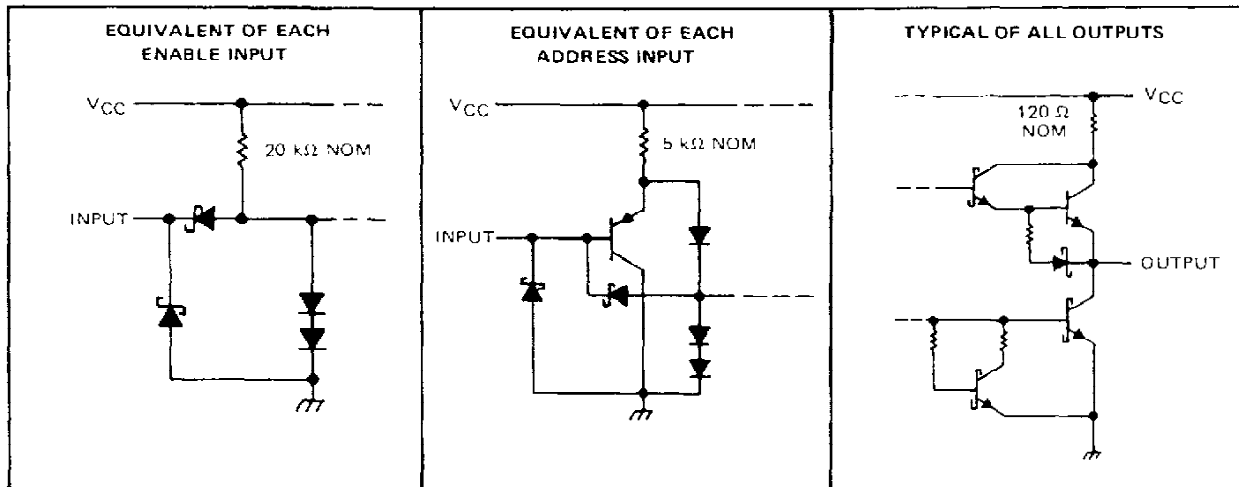
SN54LS137 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



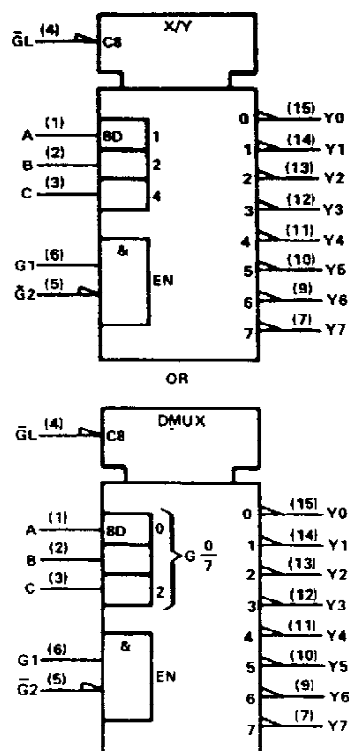
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TEXAS
INSTRUMENTS

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SN54LS137, SN74LS137 **3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS** **WITH ADDRESS LATCHES**

logic symbols†



FUNCTION TABLE

INPUTS					OUTPUTS								
ENABLE			SELECT										
GL	G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address. L: all others, H							

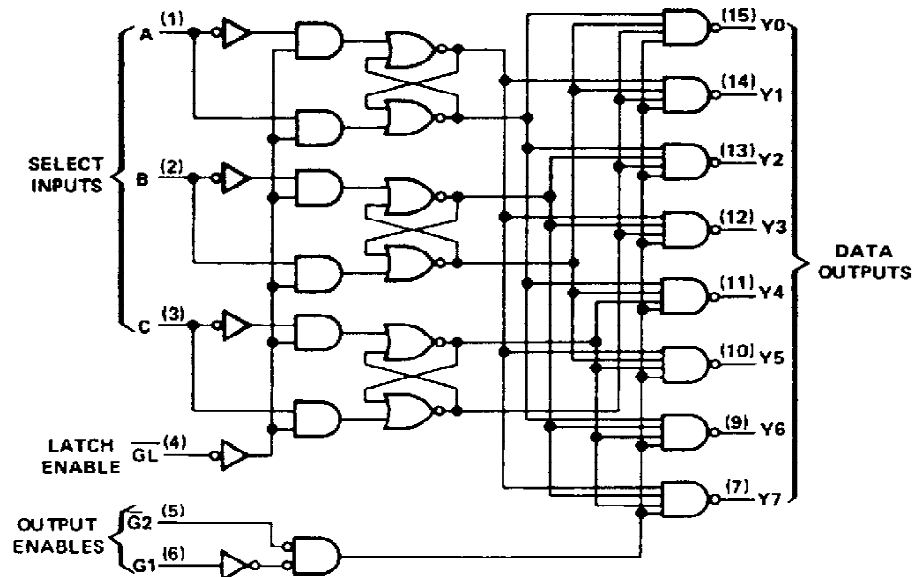
H = high level, L = low level, X = irrelevant

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS137, SN74LS137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS
WITH ADDRESS LATCHES

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS137	-55°C to 125°C
SN74LS137	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS137, SN74LS137 **3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS** **WITH ADDRESS LATCHES**

recommended operating conditions

	SN54LS137			SN74LS137			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse at $\overline{G_L}$, t_w	15			15			ns
Setup time at A, B, and C inputs, t_{su}	10			10			ns
Hold time at A, B, and C inputs, t_h	10			10			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS137		SN74LS137		UNIT		
			MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IH}	High-level input voltage		2			2		V	
V _{IL}	Low-level input voltage				0.7		0.8	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5	V	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 μA	2.5	3.5		2.7	3.5	V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max		0.25	0.4		0.25	0.4	V
						0.35	0.5		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20		20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA	
			Enable A, B, C		-0.2		-0.2		
I _{OS}	Short-circuit output current‡	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2		11	18		11	18	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, see note 3

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C	Y	2	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 3	11	17	ns	
t_{PHL}			4		25	38		
t_{PLH}	A, B, C	Y	3		16	24	ns	
t_{PHL}			3		19	29		
t_{PLH}	Enable $\overline{G_2}$	Y	2		13	21	ns	
t_{PHL}			2		16	27		
t_{PLH}	Enable G_1	Y	3		14	21	ns	
t_{PHL}			3		18	27		
t_{PLH}	Enable $\overline{G_L}$	Y	3		18	27	ns	
t_{PHL}			4		25	38		

† t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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