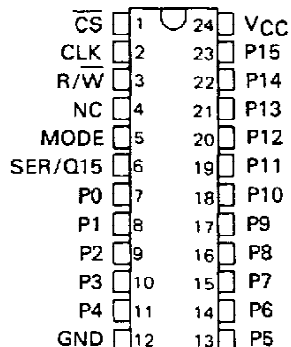


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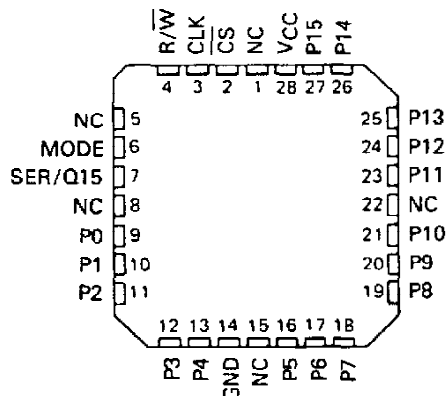
SN54LS673, SN54LS674, SN74LS673, SN74LS674

16-BIT SHIFT REGISTERS

SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS674 . . . FK PACKAGE
(TOP VIEW)



'LS673
FUNCTION TABLE

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
CS	R/W	SH CLK	STRCLR	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

'LS674 FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
CS	R/W	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

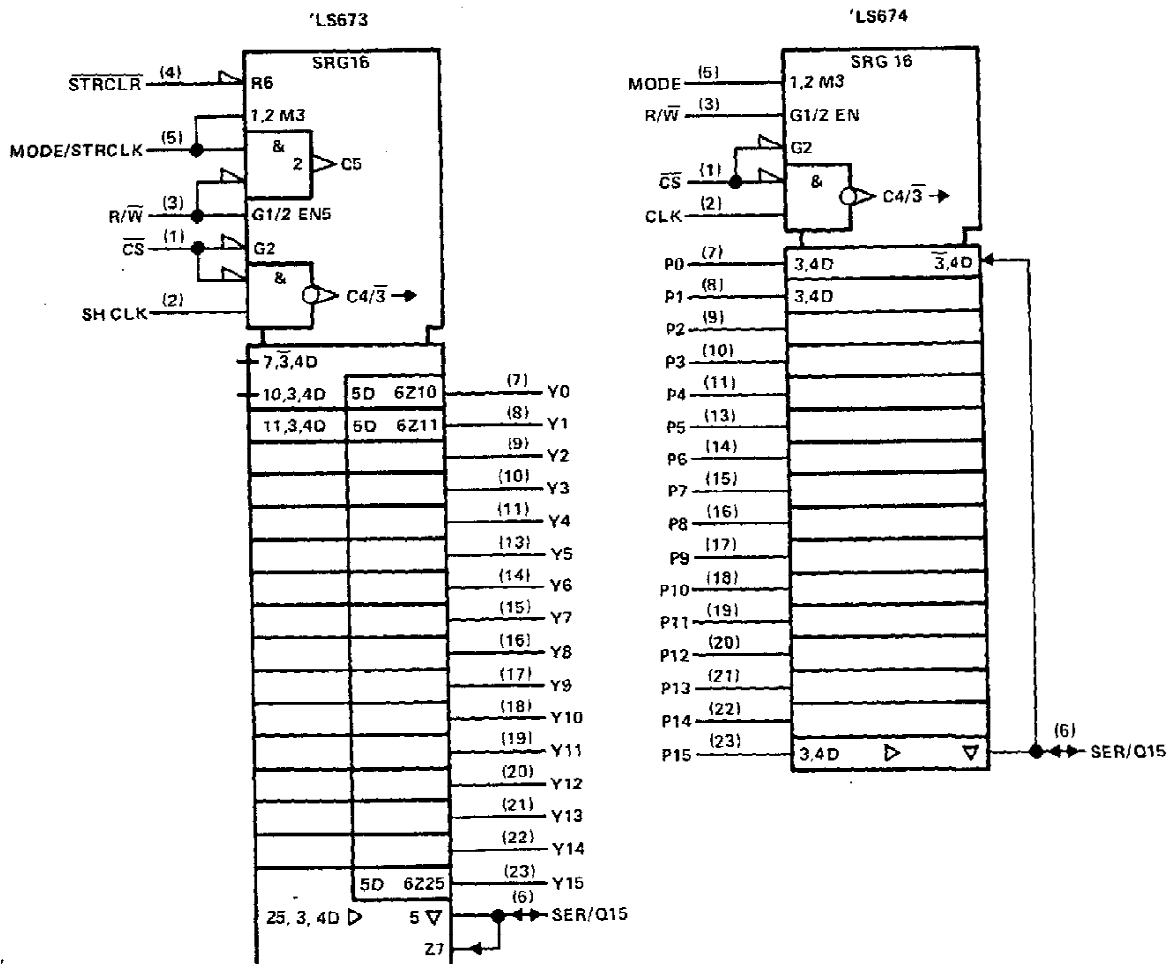
H = high level (steady state)
L = low level (steady state)
↓ = transition from low to high level
↑ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

TEXAS
INSTRUMENTS

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SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

logic symbols†

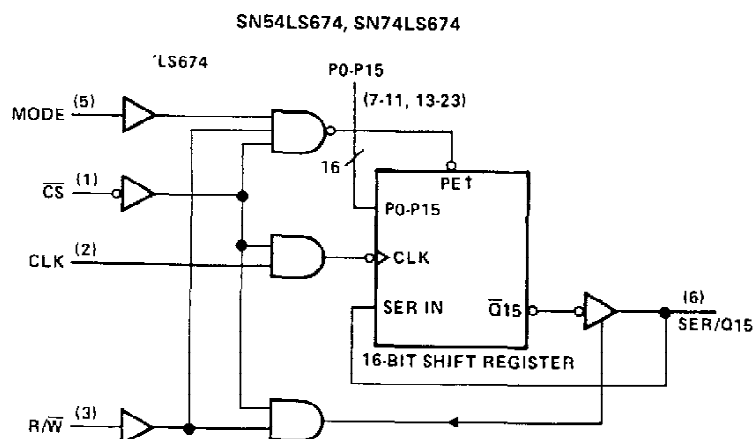
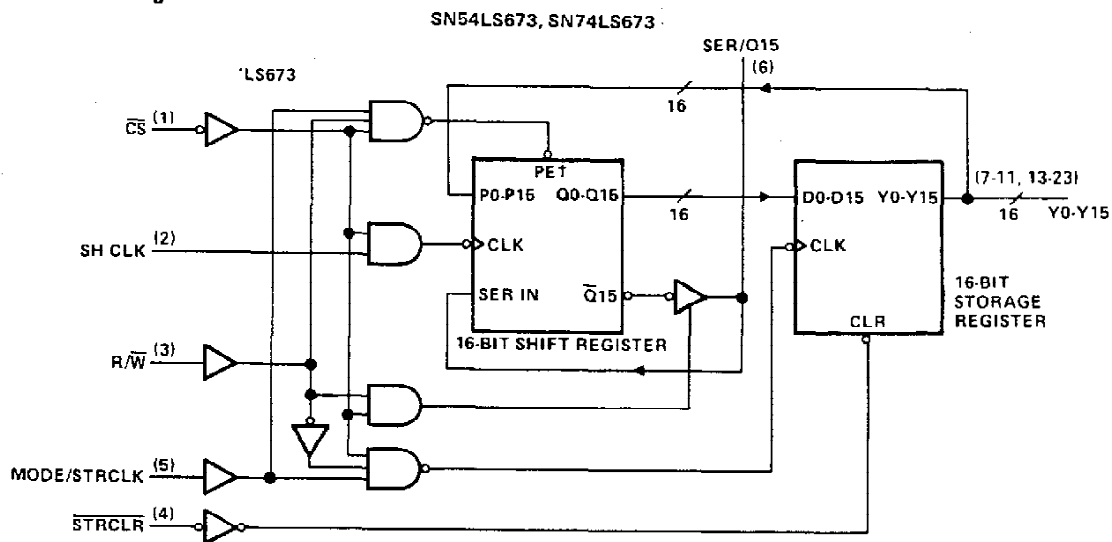


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

TEXAS
INSTRUMENTS

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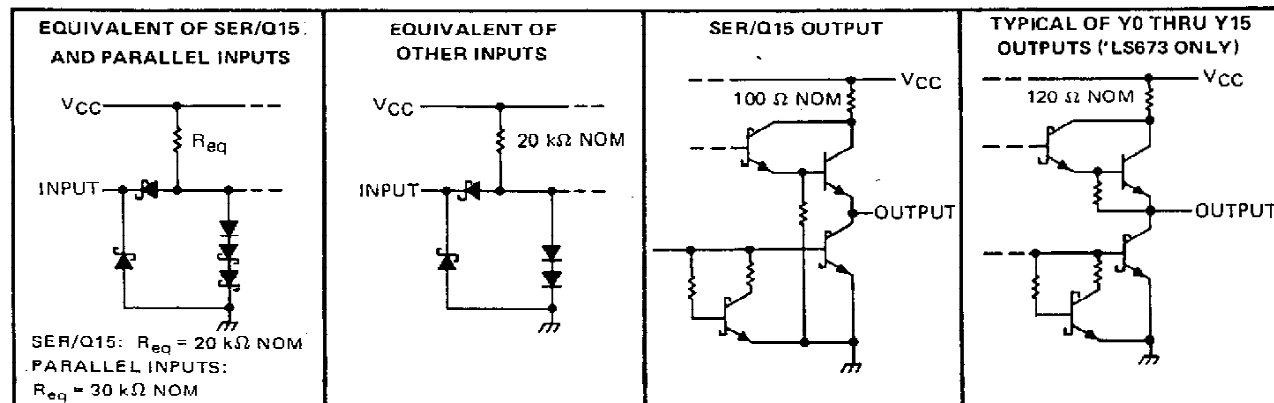
functional block diagrams



†When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place. Pin numbers shown are for DW, J, N, and W packages.

SN54LS673, SN54LS674, SN74LS673, SN74LS674
16-BIT SHIFT REGISTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: SER/Q15	5.5 V
All others	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674	–55°C to 125°C
SN74LS673, SN74LS674	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current	SER/Q15		-1			-2.6			mA
		Y0 thru Y15		-0.4			-0.4			
I _{OL}	Low-level output current	SER/Q15		12			24			mA
		Y0 thru Y15		4			8			
f _{clock}	Clock frequency			0	20		0	20		MHz
t _{w(clock)}	Width of clock input pulse			20			20			ns
t _{w(clear)}	Width of clear input pulse			20			20			ns
t _{su}	Setup time	SER/Q15		20			20			ns
		P0 thru P15		20			20			
		Mode		35			35			
		R/W, CS		35			35			
		SH CLK ↑ to Mode/STR CLK ↑ See Note 2		25			25			
t _h	Hold time	SER/Q15		0			0			ns
		P0 thru P15	'LS673	0			0			
			'LS674	5.0			5.0			
		Mode		0			0			
T _A	Operating free-air temperature			-55	125		0	70		°C

NOTE 2: This setup time ensures the storage register will see stable data from the shift register.

SN54LS673, SN54LS674, SN74LS673, SN74LS674

16-BIT SHIFT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT
			MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage		0.7		0.8		V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA	-1.5		-1.5		V
V _{OH}	High-level output voltage	SER/Q15	V _{CC} = MIN, V _{IH} = 2 V,		2.4 3.2		V
		Y0 thru Y15¶	V _{IL} = V _{ILmax} , I _{OH} = MAX		2.5 3.4		
V _{OL}	Low-level output voltage	SER/Q15	V _{CC} = MIN, V _{IH} = 2 V,	I _{OL} = 12 mA	0.25 0.4		V
				I _{OL} = 24 mA	0.35 0.5		
		Y0 thru Y15¶	V _{IL} = V _{ILmax}	I _{OL} = 4 mA	0.25 0.4		
				I _{OL} = 8 mA	0.35 0.5		
I _{OZH}	Off-state output current, high-level voltage applied	SER/Q15	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 2.7 V		40		µA
I _{OZL}	Off-state output current, low-level voltage applied	SER/Q15	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 0.4 V		- 0.4		mA
I _I	Input current at maximum input voltage	SER/Q15	V _{CC} = MAX	V _I = 5.5 V	0.1		mA
		Others		V _I = 7 V	0.1		
I _{IH}	High-level input current	SER/Q15	V _{CC} = MAX, V _I = 2.7 V		40		µA
		Others			20		
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4 V		-0.4		mA
I _{OS}	Short-circuit output current§	SER/Q15	V _{CC} = MAX		-30	-130	mA
		Y0 thru Y15¶			-20	-100	
I _{CC}	Supply current	'LS673	V _{CC} = MAX		50	80	mA
		'LS674			25	40	

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

¶ 'LS673 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2 :

PARAMETER	'LS673		'LS674		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	FROM	TO	FROM	TO					
f _{max}	SH CLK	SER/Q15	CLK	SER/Q15	R _L = 667 Ω, C _L = 45 pF	20	28		MHz
t _{PHL}	STRCLR	Y0 thru Y15			R _L = 2 kΩ, C _L = 15 pF		25	40	ns
t _{PLH}	MODE/	Y0 thru Y15					28	45	
t _{PHL}	STRCLK						30	45	
t _{PLH}	SH CLK	SER/Q15	CLK	SER/Q15	R _L = 667 Ω, C _L = 45 pF	21	33		ns
t _{PHL}						26	40		
t _{PZH}	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R _L = 667 Ω, C _L = 45 pF	30	45		ns
t _{PZL}						30	45		
t _{PHZ}	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R _L = 667 Ω, C _L = 5 pF	25	40		ns
t _{PLZ}						25	40		

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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