

SN54S182, SN74S182 LOOK-AHEAD CARRY GENERATORS

SDLS206

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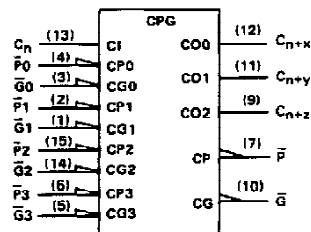
- Directly Compatible for Use With:
SN54LS181/SN74LS181,
SN54S281/SN74S281, SN54S381,
SN74S381, SN54S481/SN74S481

PIN DESIGNATIONS

ALTERNATIVE DESIGNATIONS†	PIN NOS.	FUNCTION
$\bar{G}0, \bar{G}1, \bar{G}2, \bar{G}3$	3, 1, 14, 5	CARRY GENERATE INPUTS
$P0, P1, P2, P3$	4, 2, 15, 6	CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	CARRY OUTPUTS
\bar{G}	10	CARRY GENERATE OUTPUT
P	7	CARRY PROPAGATE OUTPUT
VCC	16	SUPPLY VOLTAGE
GND	8	GROUND

†Interpretations are illustrated in the 'LS181, 'S181 data sheet.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

description

The SN54S182 and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

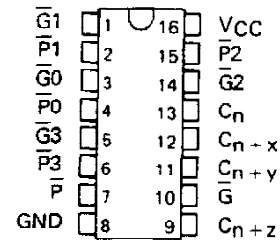
When used in conjunction with the 'LS181 or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each 'S182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading 'S182 circuits to perform multilevel look-ahead is illustrated under typical application data.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the 'LS181 and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 'S182 are:

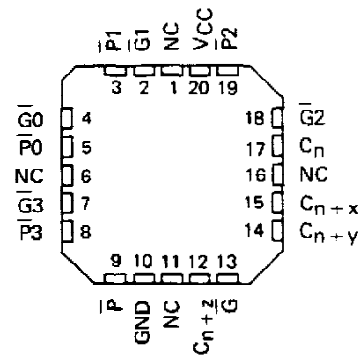
$$\begin{aligned} C_{n+x} &= G0 + P0 C_n \\ C_{n+y} &= G1 + P1 G0 + P1 P0 C_n \\ C_{n+z} &= G2 + P2 G1 + P2 P1 G0 + P2 P1 P0 C_n \\ \bar{G} &= \bar{G}3 + P3 G2 + P3 P2 G1 + P3 P2 P1 G0 \\ P &= P3 P2 P1 P0 \end{aligned}$$

$$\begin{aligned} \bar{C}_{n+x} &= \bar{Y0} (X0 + C_n) \\ \bar{C}_{n+y} &= \bar{Y1} [X1 + Y0 (X0 + C_n)] \\ \bar{C}_{n+z} &= \bar{Y2} \{ X2 + Y1 [X1 + Y0 (X0 + C_n)] \} \\ Y &= Y3 (X3 + Y2) (X3 + X2 + Y1) (X3 + X2 + X1 + Y0) \\ X &= X3 + X2 + X1 + X0 \end{aligned}$$

SN54S182 . . . J OR W PACKAGE
SN74S182 . . . D OR N PACKAGE
(TOP VIEW)



SN54S182 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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FUNCTION TABLE FOR \bar{G} OUTPUT

INPUTS							OUTPUT \bar{G}
\bar{G}_3	\bar{G}_2	\bar{G}_1	\bar{G}_0	\bar{P}_3	\bar{P}_2	\bar{P}_1	
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE
FOR \bar{P} OUTPUT

INPUTS				OUTPUT \bar{P}
\bar{P}_3	\bar{P}_2	\bar{P}_1	\bar{P}_0	
L	L	L	L	L
All other combinations				H

FUNCTION TABLE
FOR C_{n+x} OUTPUT

INPUTS			OUTPUT C_{n+x}
\bar{G}_0	\bar{P}_0	C_n	
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE
FOR C_{n+y} OUTPUT

INPUTS					OUTPUT C_{n+y}
\bar{G}_1	\bar{G}_0	\bar{P}_1	\bar{P}_0	C_n	
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

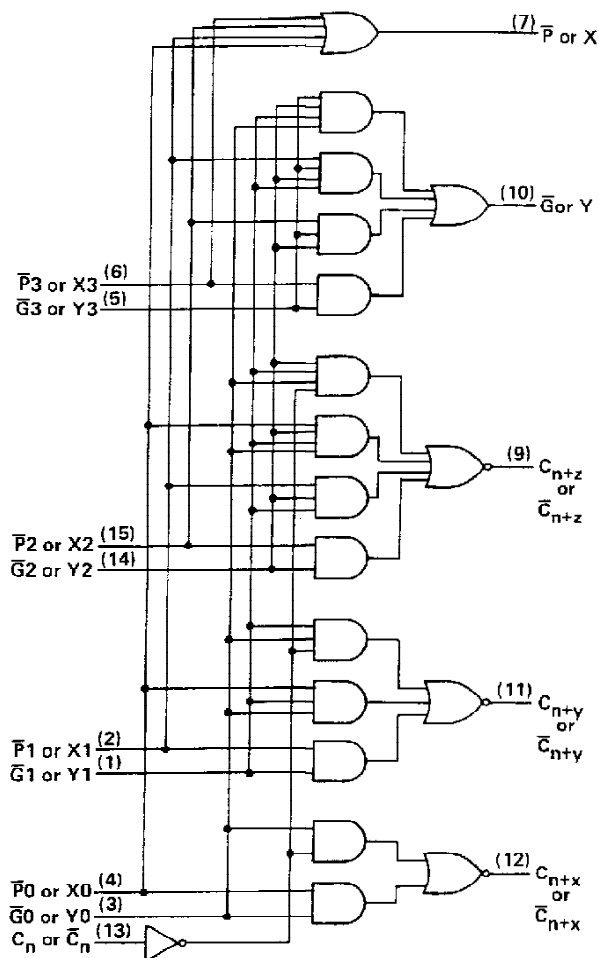
FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT C_{n+z}
\bar{G}_2	\bar{G}_1	\bar{G}_0	\bar{P}_2	\bar{P}_1	\bar{P}_0	C_n	
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high level, L = low level, X = irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)



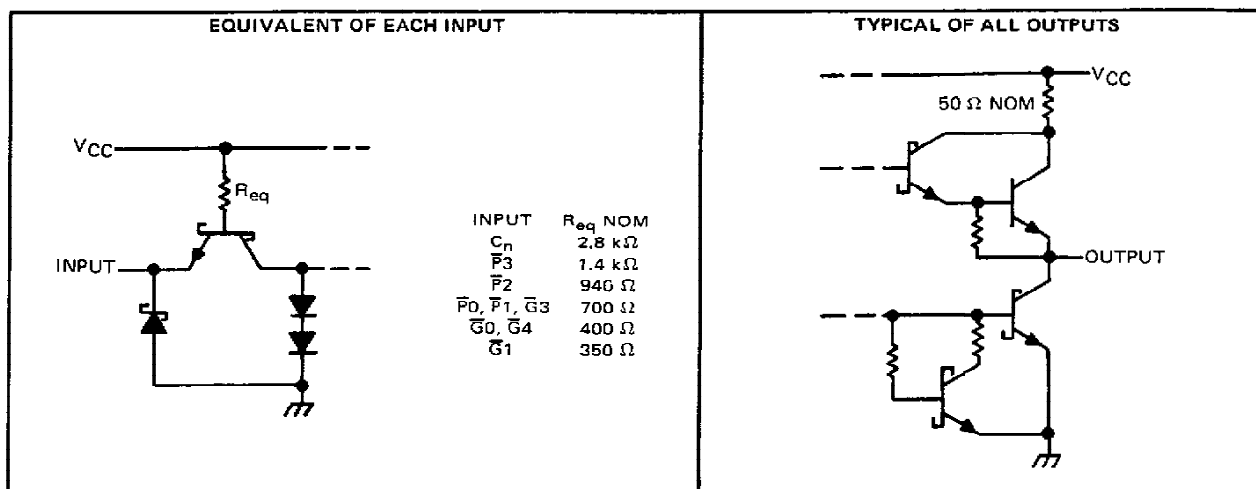
Pin numbers shown are for D, J, N, and W packages.

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54S182	-55°C to 125°C
SN74S182	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter input transistor. For these circuits, this rating applies to each \bar{G} input in conjunction with any other \bar{G} input or in conjunction with any \bar{P} input.

SN54S182, SN74S182 LOOK-AHEAD CARRY GENERATORS

recommended operating conditions

	SN54S182			SN74S182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S182			SN74S182			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN.}$ $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX.}$ $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	C_n input			50			50	μA
		$\bar{P}3$ input			100			100	
		$\bar{P}2$ input			150			150	
		$\bar{P}0, \bar{P}1$, or $\bar{G}3$ input			200			200	
		$\bar{G}0$ or $\bar{G}2$ input			350			350	
		$\bar{G}1$ input			400			400	
I_{IL}	Low-level input current	C_n input			-2			-2	mA
		$\bar{P}3$ input			-4			-4	
		$\bar{P}2$ input			-6			-6	
		$\bar{P}0, \bar{P}1$, or $\bar{G}3$ input			-8			-8	
		$\bar{G}0$ or $\bar{G}2$ input			-14			-14	
		$\bar{G}1$ input			-16			-16	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX.}$	-40		-100	-40		-100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC} = 5 \text{ V}$, See Note 3	35	65		35	70		mA
I_{CCL}	Supply current, all outputs low	$V_{CC} = \text{MAX.}$, See Note 4	69	99		69	109		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTES: 3. I_{CCH} is measured with all outputs open, inputs $\bar{P}3$ and $\bar{G}3$ at 4.5 V, and all other inputs grounded. MAX is determined at 5.5 V.

4. I_{CCL} is measured with all outputs open; inputs $\bar{G}0$, $\bar{G}1$, and $\bar{G}2$ at 4.5 V; and all other inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

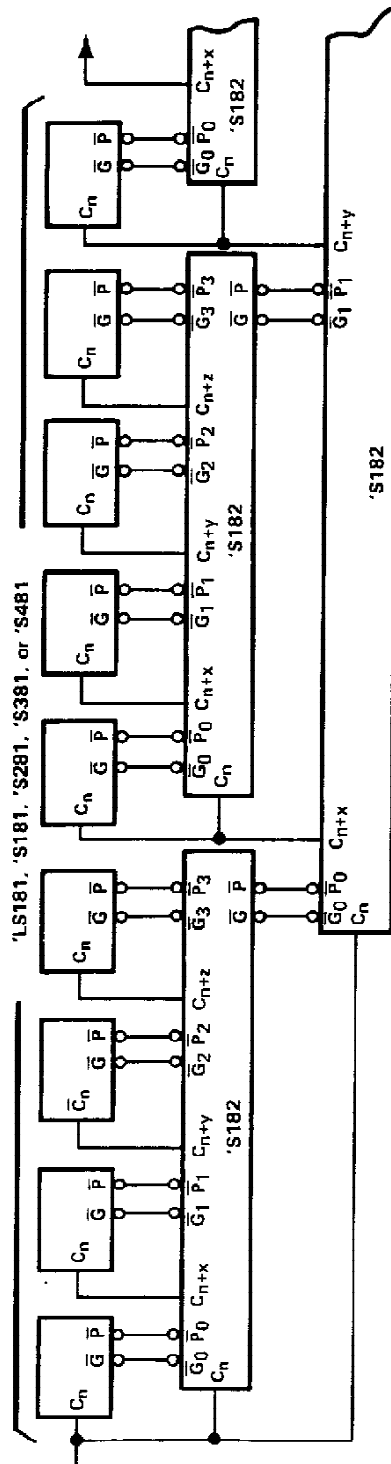
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$\bar{G}0, \bar{G}1, \bar{G}2, \bar{G}3$	C_{n+x}, C_{n+y} , or C_{n+z}	$R_L = 280 \Omega$, $C_L = 15 \text{ pF}$, See Note 5	4.5	7		ns
t_{PHL}	$P0, P1, P2$, or $P3$			4.5	7		
t_{PLH}	$\bar{G}0, \bar{G}1, \bar{G}2, \bar{G}3$	\bar{G}		5	7.5		ns
t_{PHL}	$P1, P2$, or $P3$			7	10.5		
t_{PLH}	$\bar{P}0, \bar{P}1, \bar{P}2$, or $\bar{P}3$	\bar{P}		4.5	6.5		ns
t_{PHL}				6.5	10		
t_{PLH}	C_n	C_{n+x}, C_{n+y} , or C_{n+z}		6.5	10		ns
t_{PHL}				7	10.5		

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

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TYPICAL APPLICATION DATA



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

Remaining inputs and outputs of 'LS181, 'S181, 'S281, 'S381, and 'S481 are not shown.

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