

TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN54LS90, SN54LS92, SN54LS93, SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

MARCH 1974 — REVISED DECEMBER 1983

'90A, 'L90, 'LS90 ... DECADE COUNTERS

'92A, 'LS92 ... DIVIDE-BY-TWELVE COUNTERS

'93A, 'L93, 'LS93 ... 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW
'L93	16 mW

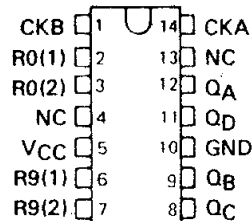
description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

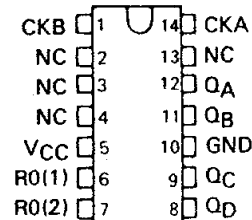
All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A .

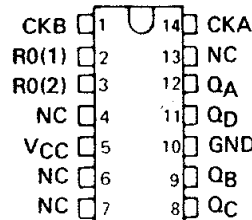
SN5490A, SN54LS90 ... J OR W PACKAGE
SN54L90 ... J PACKAGE
SN7490A ... J OR N PACKAGE
SN74LS90 ... D, J OR N PACKAGE
(TOP VIEW)



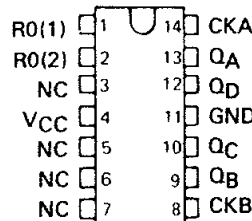
SN5492A, SN54LS92 ... J OR W PACKAGE
SN7492A ... J OR N PACKAGE
SN74LS92 ... D, J OR N PACKAGE
(TOP VIEW)



SN5493A, SN54LS93 ... J OR W PACKAGE
SN7493A ... J OR N PACKAGE
SN74LS93 ... D, J OR N PACKAGE
(TOP VIEW)



SN54L93 ... J PACKAGE
(TOP VIEW)



NC - No internal connection

For new chip carrier design, use
'LS290, 'LS292, and 'LS293.

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PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**TYPES SN5490A, '92A, '93A, SN54L90, 'L93, SN54LS90, 'LS92, 'LS93,
SN7490A, '92A, '93A, SN74LS90, 'LS92, 'LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

**'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)**

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**'92A, 'LS92
COUNT SEQUENCE
(See Note C)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

**'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE**

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

**'93A, 'L93, 'LS93
COUNT SEQUENCE
(See Note C)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

**'92A, 'LS92, '93A, 'L93, 'LS93
RESET/COUNT FUNCTION TABLE**

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

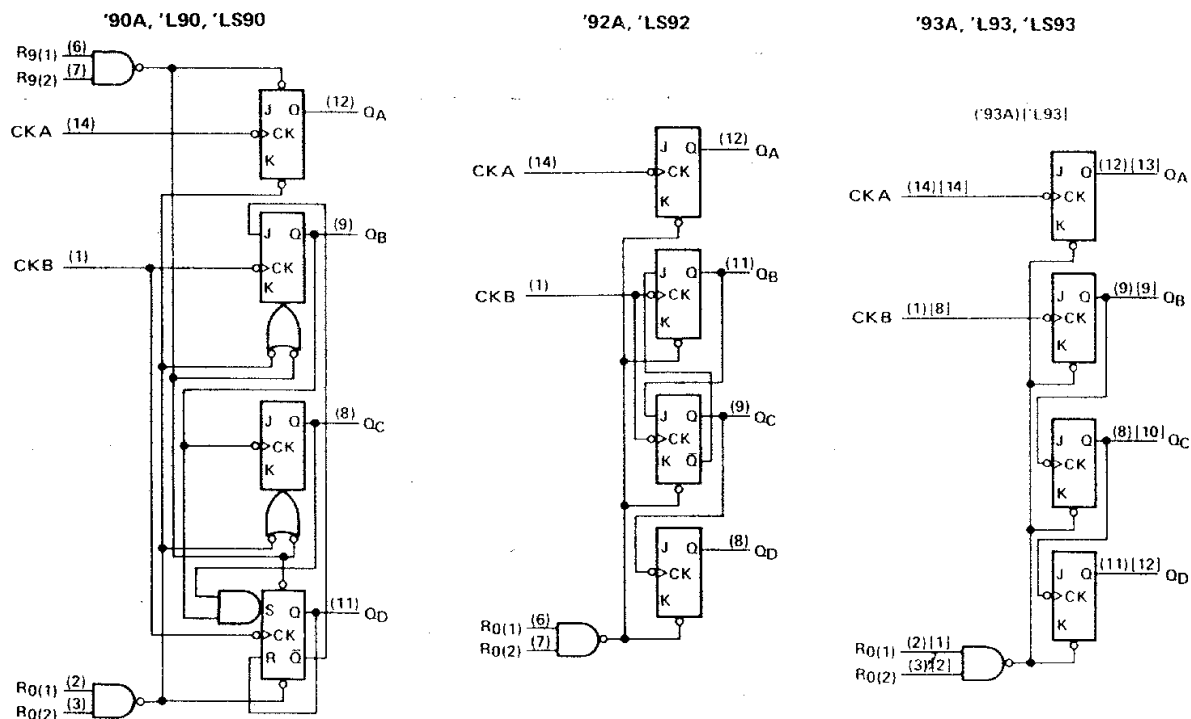
NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.
C. Output Q_A is connected to input CKB.
D. H = high level, L = low level, X = irrelevant

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TTL DEVICES

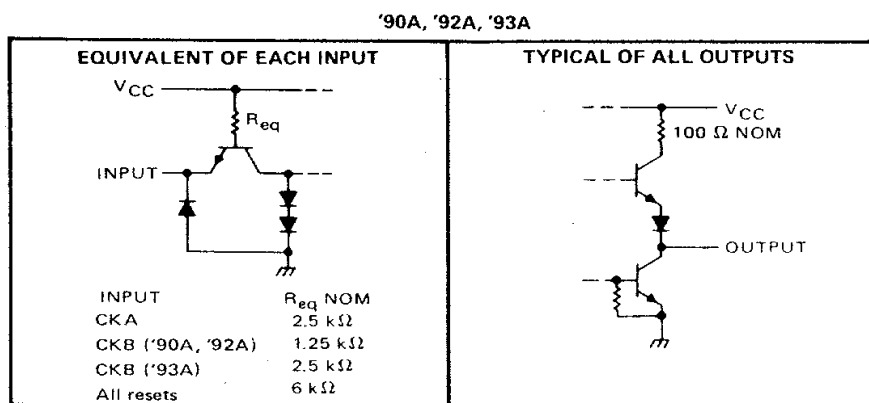
TYPES SN5490A, '92A, '93A, SN54L90, 'L93, SN54LS90, 'LS92, 'LS93 SN7490A, '92A, '93A, SN74LS90, 'LS92, 'LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

logic diagrams



The J and K inputs shown without connection are for reference only and are functionally at a high level. Pin numbers shown in [] are for the 'LS93 and '93A and pin numbers shown in () are for the 54L93.

schematics of inputs and outputs



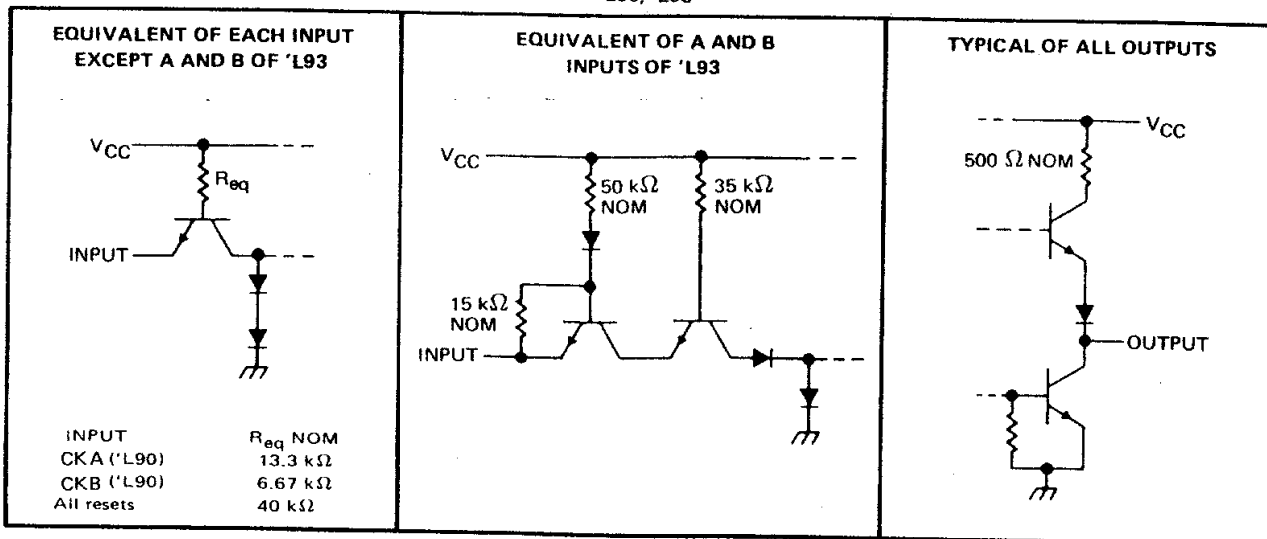
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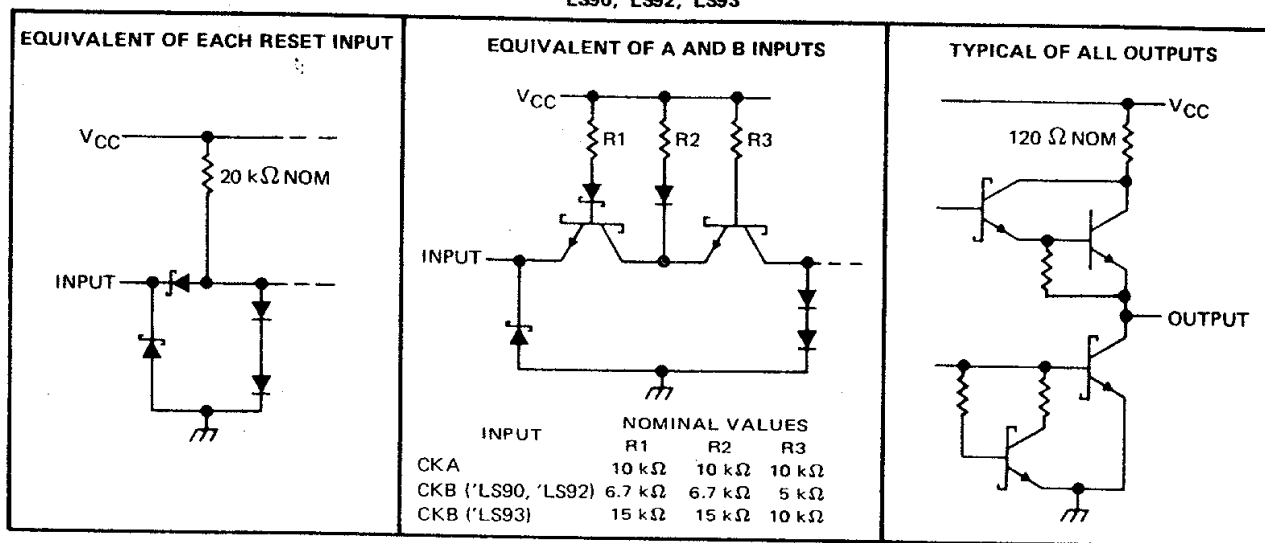
**TYPES SN54L90, 'L93, SN54LS90, 'LS92, 'LS93
SN74LS90, 'LS92, 'LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

schematics of inputs and outputs (continued)

'L90, 'L93



'LS90, 'LS92, 'LS93



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TTL DEVICES

TYPES SN5490A, SN5492A, SN5493A, SN7490A, SN7492A, SN7493A DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A	-55°C to 125°C
SN7490A, SN7492A, SN7493A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor. For these circuits, this rating applies between the two R_G inputs, and for the '90A circuit, it also applies between the two R_G inputs.

recommended operating conditions

		SN5490A, SN5492A SN5493A			SN7490A, SN7492A SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{SU}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER [¶]		TEST CONDITIONS [†]		'90A			'92A			'93A			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$				-1.5			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}^{\S}$			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$				1			1			1	mA
I_{IH}	High-level input current	Any reset				40			40			40	μ A
		CKA	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			80			80			80	
		CKB				120			120			80	
I_{IL}	Low-level input current	Any reset				-1.6			-1.6			-1.6	mA
		CKA	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-3.2			-3.2			-3.2	
		CKB				-4.8			-4.8			-3.2	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54 [¶]	-20		-57	-20		-57	-20		-57	mA
			SN74 [¶]	-18		-57	-18		-57	-18		-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3		29	42		26	39		26	39		mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

[¶] Q_A outputs are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_G inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

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TTL DEVICES

TYPES SN5490A, SN5492A, SN5493A, SN7490A, SN7492A, SN7493A DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{\max}	CKA	Q_A	$C_L = 15\text{ pF},$ $R_L = 400\ \Omega,$ See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q_B		16			16			16			
t_{PLH}	CKA	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	CKA	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	CKB	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	CKB	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	CKB	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	40							

¹ f_{\max} maximum count frequency

t_{PLH} propagation delay time, low-to-high-level output

t_{PHL} propagation delay time, high-to-low-level output

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TTL DEVICES

TYPES SN54L90, SN54L93 DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	8 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range:	-55°C to 125°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54L90, SN54L93			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
f_{count}	Count frequency	0		3	MHz
I_{OH}	High-level output current			-0.1	mA
I_{OL}	Low-level output current			2	mA
$t_w(count)$	Width of input count pulse	200			ns
$t_w(reset)$	Width of reset pulse	200			ns
T_A	Operating free-air temperature	-55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L90			SN54L93			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OH} = \text{MAX}$	2.4		3.3	2.4		3.3	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OL} = \text{MAX}^{\S}$	0.15		0.3	0.15		0.3	V
I_I	Input current at maximum input voltage	Any reset input			100			100	μA
		CKA			300			200	
		CKB			600			200	
I_{IH}	High-level input current	Any reset input			10			10	μA
		CKA			30			20	
		CKB			60			20	
I_{IL}	Low-level input current	Any reset input			-0.18			-0.18	mA
		CKA			-0.54			-0.36	
		CKB			-1.08			-0.36	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-3		-15	-3		-15	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3	4		7.2	3.2		6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

¶ I_{OH} outputs are tested at $I_{OL} = \text{MAX}$ plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	SN54L90			SN54L93			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum count frequency		3	6		3	6		MHz
t_{PLH}	Propagation delay time, low-to-high-level Q_D output from input CKA	$C_L = 50 \text{ pF}, R_L = 4 \text{ k}\Omega$, See Figure 1	230	340		280	450		ns
t_{PHL}	Propagation delay time, high-to-low-level Q_D output from input CKB		230	340		280	450		ns

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