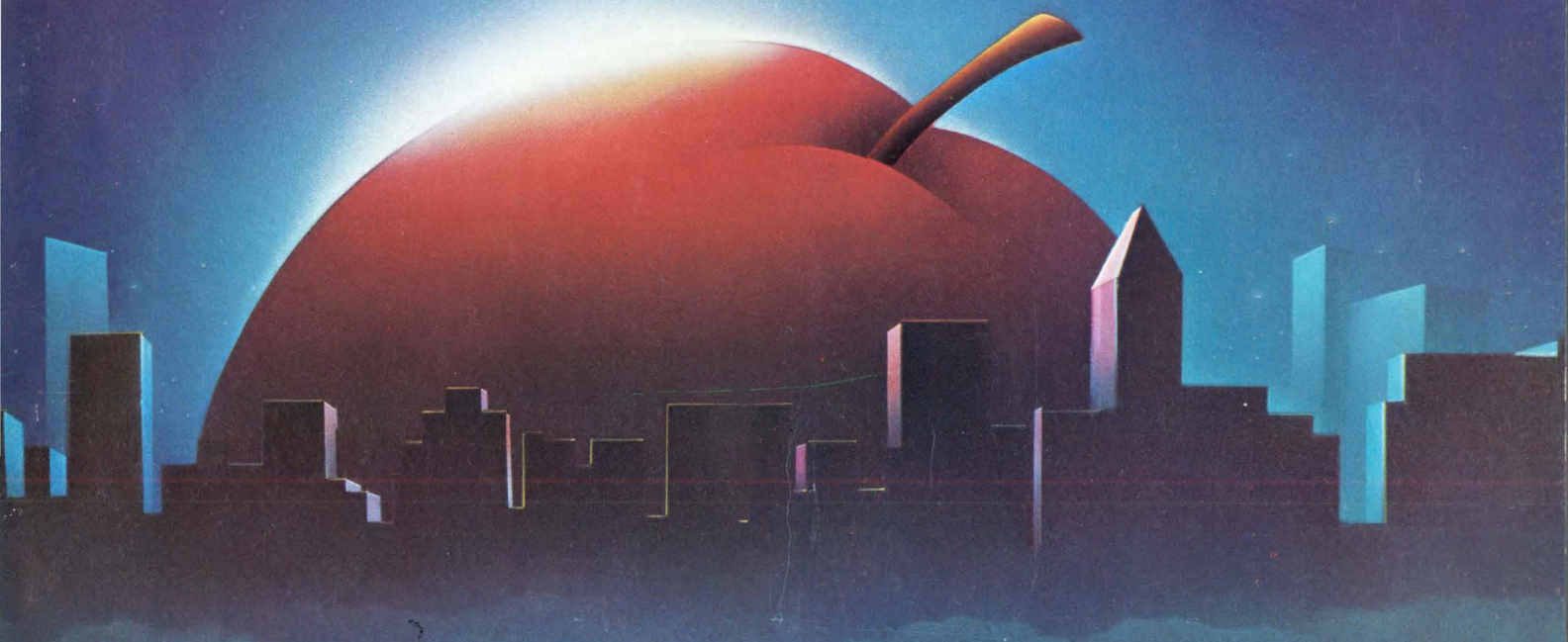
VOLUME 9, NO. 5

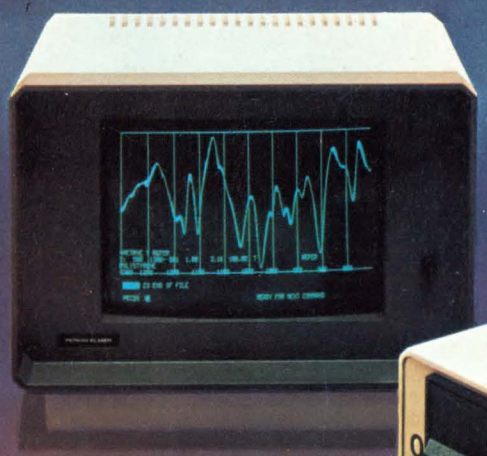
NCC'79 PREVIEW

MAY 1979

Digital Design

The Magazine of Systems Electronics





Data Acquisition and Conversion

µP Development Lab

µC Software

Fiber Optic Kits

erating Systems

ANNOUNCING–THE POWERFUL, NEW FPS-100 ARITHMETIC PROCESSOR–FOR THE OEM.

EIGHT MILLION FLOATING-POINT OPERATIONS PER SECOND... PRICE: $16,728*

A NEW LEVEL OF COST/PERFORMANCE FOR THE OEM is now available from the leader in array processing — FLOATING POINT SYSTEMS. If your application demands maximum floating-point compute power — but at minimal system cost — the FPS-100 Arithmetic Processor can satisfy your need.

EIGHT MILLION FLOATING POINT OPERATIONS PER SECOND is achieved through a unique pipelined parallel synchronous architecture. In each 250nsec cycle the FPS-100 can produce one multiply result and one add result. And with 38-bits of precision — over eight decimal digits of accuracy!

A FULL COMPLEMENT OF PROVEN SOFTWARE is available including FORTRAN Compiler, Assembler, Simulator, Debugger, Math Library — with more than 250 routines, Signal Processing Library, a Vector Function Chainer, and the APEX host executive.

SUPER-100, A NEW RESIDENT REAL-TIME OPERATING SYSTEM introduces a new dimension to array processing. Prioritized multi-tasking and extensive services permit maximum utilization of the FPS-100. The FPS-100 with the optional Super-100 and priority interrupt structure can easily accommodate demanding real-time applications.

COMPACT and completely self-contained, the FPS-100 is only 10.5" high for quick integration into your system cabinet.

ECONOMICAL HIGH PERFORMANCE COMPUTING is now within your reach — the FPS-100 can be attached easily to a small host mini to create a Super Computer System for mathematically intensive calculations.

Contact your nearest FPS representative for more details or call Jim Strelchun, (503) 641-3151.

*OEM Quantity 100 (minimum 20 units).

FLOATING POINT SYSTEMS, INC.

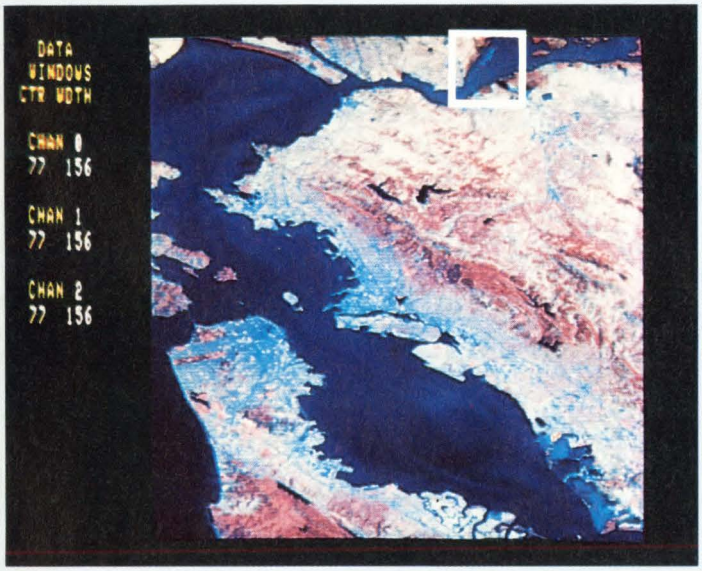
P.O. Box 23489, Portland, OR 97223
(503) 641-3151, TLX: 360470 FLOATPOINT PTL

FPS Sales and Service Worldwide: Boston, Chicago, Dallas, Denver, Detroit, Houston, Huntsville, Los Angeles, New York Orlando, Ottawa, Philadelphia, Phoenix, Portland, San Francisco, Washington, D.C. International offices: Geneva, London, Munich, Paris, Tel Aviv (Eastronix, Ltd.), Tokyo (Hakuto Co. Ltd.)

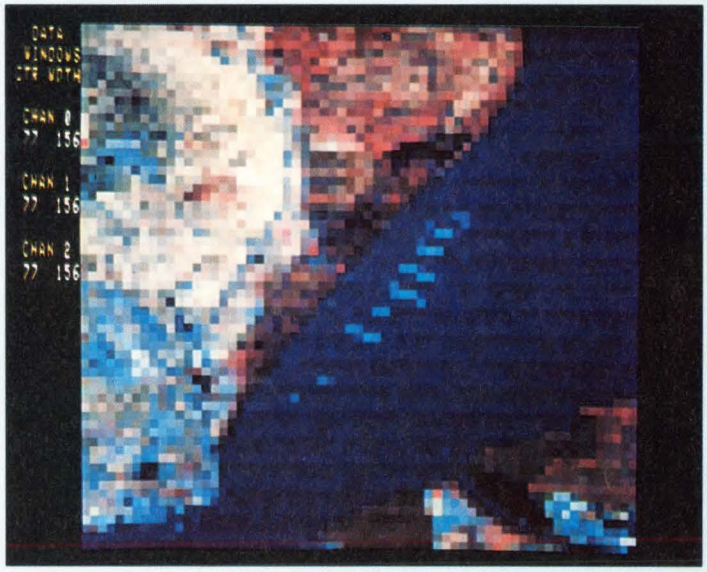
See us at NCC
Island 2231
June 4-7

Circle 120 on Reader Inquiry Card

THE IMAGE ARRAY PROCESSING SYSTEM



Three band LANDSAT image of San Francisco Bay



Eight-to-one zoom of Suisun Bay

If image analysis and aquisition is your problem, you need the IP 5000 Image Array Processor.

The display system that:

- Stores up to one megabyte of data for single or multiple image arrays.
- Has complete independence between refresh memory (raster scan output) and host computer addressability of memory.
- Includes memory management and data control for direct high speed access to refresh memory.
- Includes a powerful, pipe-line processor to perform high speed image array processing and statistical analysis.
- Performs pixel replica zoom of 2:1, 4:1 or 8:1 in real time.
- Can selectively change format between 525 line and 559 line video formats with external sync capability for 525 line formats.
- Is capable of scrolling, in any direction, a pixel or line at a time or multiple pixels and lines without causing tearing of the visible image.
- Digitizes video signals up to 8-megahertz bandwidth with true 8-bit precision.
- Has multiple intensity transformation tables for grey scale, color or pseudo color displays.
- Has proven reliability with field installation at some of the top names involved in image processing and display.

For further information and a list of satisfied users, contact DeAnza Systems, Inc., 118 Charcot Ave., San Jose, CA., 95131, (408) 263-7155.

De Anza Systems Incorporated

GIVE YOURSELF A BETTER IMAGE

Circle 19 on Reader Inquiry Card.

Introducing the Sperry
Designed exclusively for three

The Sperry Univac V77-800 Miniframe is the newest and most powerful mini we've ever built—a high performance, multi-use, general-purpose minicomputer system designed for both commercial and scientific data processing. It has a memory range from 128K bytes to 2 megabytes (with error correcting memory) and a 150 nanosecond CPU with integrated cache of 1024 bytes. Plus 12K bytes of user programmable writable control store.

There's an optional new high speed 64-bit floating point processor that works in conjunction with a new globally optimized ANS '77 FORTRAN.

No wonder our three most important customers think so highly of it.

OUR OEM CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

The Miniframe is customer microprogrammable. So an OEM can implement his own firmware packages. And with the many software packages we offer, the OEM can add all the bells and whistles he wants.

The Miniframe comes with our largest instruction set ever. So OEM's with their own software have much more flexibility in design.

The Miniframe speaks PASCAL, the powerful new language for scientific, commercial, and system programming that most competitive systems still can't speak. And of course, it also speaks COBOL, FORTRAN and RPGII.

More good news is that the Miniframe is compatible with the rest of the V77 product line.

OUR SYSTEM HOUSE CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

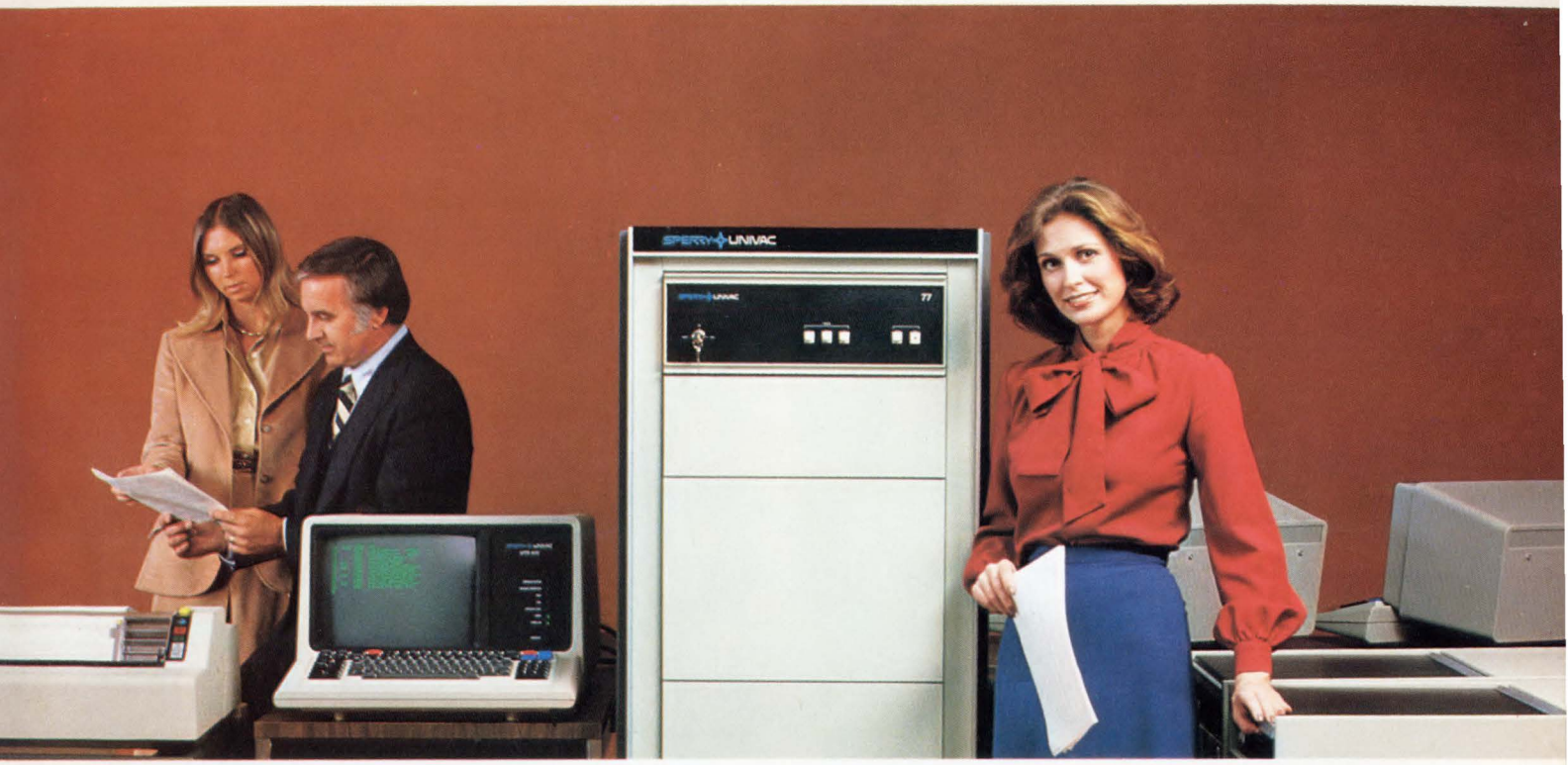
Naturally, system houses want all the features OEM's do. And more.

So we gave them more.

More operating systems, for example. Choose from VORTEX or our new SUMMIT—an interactive, multi-terminal system with transaction processing and data base management. It gives you easy editing, screen formatting, and documentation aids. Plus speedy, comprehensive program development.

System houses also think PASCAL is important. Because it's more efficient, easier to maintain, expand, and modify.

The Miniframe brings systems builders a new query language called QL-77. It features inquire and report facilities. And interfaces



Univac V77-800 Miniframe. of our very best customers.

directly to TOTAL*, the data base management system. So preprocessing and intermediate handling are a thing of the past. Finally, TOTAL also gives you complete data base access and file access security.

OUR END USER CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Take all the features we designed in for OEM's and system houses and say ditto for the end user.

But we didn't stop there. We also pressed a few special hot buttons just for end users.

Consider QL-77, for example. End users will love our new query language because it reduces the amount of application programming. By storing query language procedures right in the data base file. Where they can be easily and quickly recalled and executed at any time.

Once again, SUMMIT, our new operating system, helps the end user handle transaction processing. Without any additional, expensive software. It's also the right answer for a multi-tasking, "fully-implemented" distributed processing system.

Finally, the Miniframe supports DCA and conventional protocols. So you can talk to both SPERRY UNIVAC and IBM hosts.

YOU'LL KNOW WE DESIGNED THE MINIFRAME JUST FOR YOU.

No matter what your application, no matter what your need, the Miniframe may just be the answer.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400, ext. 536.

In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.

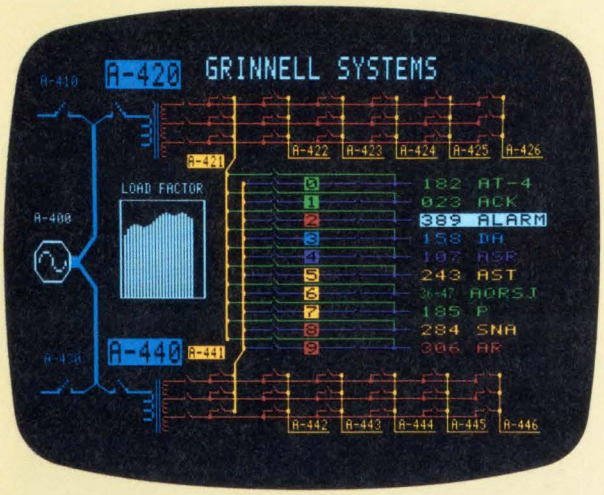
We're Sperry Univac.

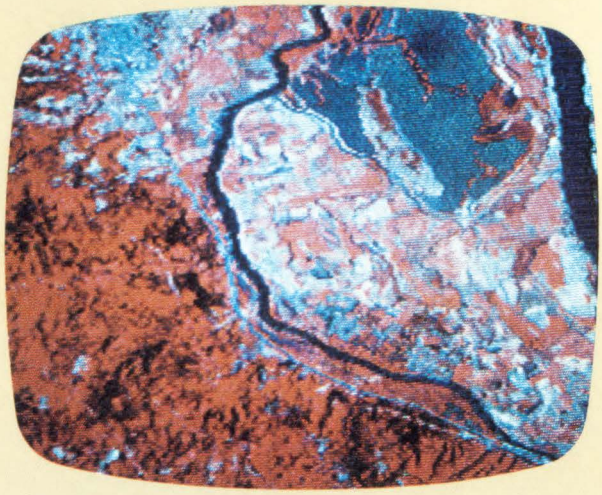
And our new Miniframe is going to solve some very big problems.

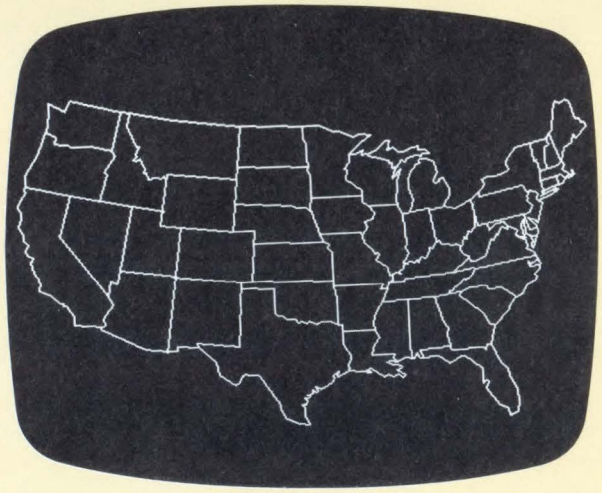
SPERRY UNIVAC

SPERRY UNIVAC IS A DIVISION OF SPERRY RAND CORPORATION

Grinnell has your display...







from low cost imaging and graphics to full color image processing

Our modular, solid state systems can meet your computer display requirement, easily and economically.

And, they're intelligent. Every system has a complete alphanumerics and graphics package, and a powerful instruction set that simplifies programming—no need for complex macro-instructions and high order programming languages.

There's also a choice of standard resolutions: 256 x 256, 256 x 512, 512 x 512 (30 Hz or 60 Hz refresh) and 1024 x 1024. Plus plug compatible interfaces for most minis.

Options include overlays, function memories, pseudo-color tables, zoom and pan, independent cursors with trackball and joystick controls, split-screen, image toggling, and real time digitizers that grab and store images and sum consecutive frames.

Grinnell displays are already used for tomography, ERTS imaging, process control, image processing, animation and much more. All systems drive standard TV monitors.

So before you choose a display system, let our experts show you how to maximize performance and minimize cost. For details, and/or a quote, call or write.

GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920

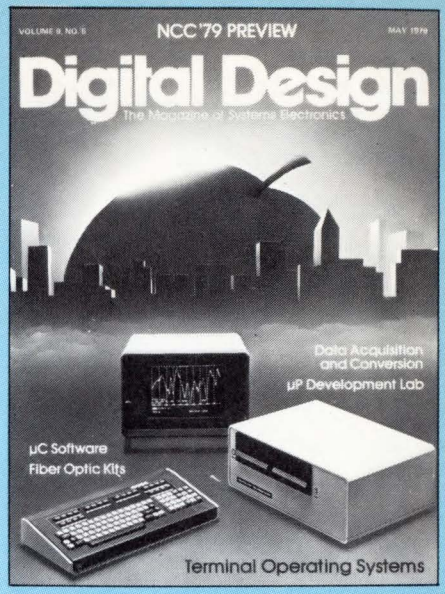
Circle 6 on Reader Inquiry Card

THIS MONTH

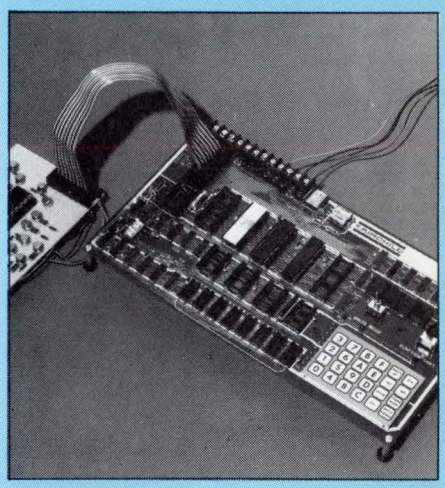
May 1979
Volume 9, No. 5

Features

Departments



ON OUR COVER
New developments in memories, computers, peripherals and communications – all these and more will be unveiled at this June's NCC in New York City. We thank Perkin-Elmer for this magazine cover portraying the Beaver's modularity.



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A Beautiful Way To Interface

IQ 140

SOROC's first and foremost concern, to design outstanding remote video displays, has resulted in the development of the IQ 140. This unit reflects exquisite appearance and performance capabilities unequaled by others on the market.

With the IQ 140, the operator is given full command over data being processed by means of a wide variety of edit, video, and mode control keys, etc.

The detachable keyboard, with its complement of 117 keys, is logically arranged into 6 sections plus main keyboard to aid in the overall convenience of operation. For example, a group of 8 keys for cursor control / 14 keys accommodate numeric entry / 16 special function keys allow access to 32 pre-programmed commands / 8 keys make up the extensive edit and clear section / 8 keys for video set up and mode control / and 8 keys control message and print.

Two Polling options available: 1) Polling compatible with Lear Siegler's ADM-2. 2) Polling discipline compatible with Burroughs.

IQ 120

The SOROC IQ 120 is the result of an industry-wide demand for a capable remote video display terminal which provides a multiple of features at a low affordable price. The IQ 120 terminal is a simple self-contained, operator / computer unit.

The IQ 120 offers such features as: 1920 character screen memory, lower case, RS232C extension, switch selectable transmission rates from 75 to 19,200 bps, cursor control, addressable cursor, erase functions and protect mode. Expansion options presently available are: block mode and hard copy capability with printer interface. The IQ 120 terminal incorporates a 12-inch, CRT formatted to display 24 lines with 80 characters per line.

SOROC TECHNOLOGY, INC.

165 FREEDOM AVE., ANAHEIM, CALIF. 92801

(714) 992-2860 / (800) 854-0147

LETTERS

AIOU is Great . . .

When we ran our editorial Speakout on open universities as an alternative to traditional universities, we had no idea of the enormity of this issue nor of the hundreds of notes, comments and letters (not to mention the calls) that we'd received from our readers. Most were against open universities (almost 85%), although the remainder felt strongly in favor of AIOU and gave very good reasons. Here is a sampling of the pro-AIOU mail...

Dear Editor:

Alternatives to the "traditional" educational system are needed and, thankfully, on the increase. To say only those who have attended traditional institutions are competent is selling ourselves short as human beings. After all, in any field of endeavor, the idea in education learn, and new, more effective ways are feasible — although not widely implemented.

B.C.D.
Landing, NJ

Dear Editor:

I thought that IEEE might be worth joining if Feerst could get elected. That was before his assinine attack on AIOU, and on the concept of any alternative to the traditional approach of the academic community....

S.T.H.
Lincoln, MA

Dear Editor:

Irwin Feerst's concern about cheapening of his "hard-earned degree" appears to be the thrust of his anxiety. But degrees do not guarantee an individual's responsibility to create and solve problems. If a degree was mandatory, some of the world's greatest problems would still be unsolved.

W.L.J.
Rochester, NY

Dear Editor:

Feerst keeps loosing because of his offensive personality and hip-shooting....

M.S.
Boonton, NJ

Dear Editor:

In reference to no exams, professionalism does not require a degree or titles, which are other means of establishing standards of knowledge. However, if achievement is to be used, rigorous attention must be exercised to maintain those standards. Otherwise, titles will become meaningless.

S.L.
Greensboro, NC

Dear Editor:

I would like to see published a list of open universities with cost, addresses and application requirements.

F.D.G.
Glenshaw, PA

Dear Editor:

I am for open universities — a piece of paper from any school does not prove one's capabilities. Good people are on both sides of this issue.

J.C.H.
Bellevue, NE

Dear Editor:

I think we should give the newly elected people in IEEE a chance to perform. However, constructive criticism is always useful.

A.H.E.
Forster City, CA

Dear Editor:

Why not distinguish between degrees received from AIOU in an engineering school by giving them different names, and allow employers to decide upon their merits? They are the ultimate judges anyway.

W.M.
Blue Belle, PA

Dear Editor:

In reference to open universities, I find that a good open university can be fine if the student's aim is to learn something. A diploma mill can be very bad, though.

P.L.S.
Carlsbad, CA

AIOU hurts Us . . .

On the reverse side of this issue, many readers were incensed at the concept of open universities and really let us know. One reader even wrote to us about how the International Entrepreneurs' Association recommends open universities as a low-cost business that can make its founders big profits. This reader even included an IEA booklet that explained how IEA could provide instructions for starting your own university with "exact step-by-step details...exact cost...how much profit to expect and when...and how to avoid all the pitfalls...advertising and promotion...how to locate customers for your open university..." Another reader wrote to us and told how he had visited AIOU headquarters and saw only one piece of lab equipment — a xerox machine! So, we thought you'd like to see a sampling of the anti-AIOU mail...

Dear Editor:

I would have spent 15¢ if for no other reason than to tell you how much I disapprove of so-called open universities; all they succeed in doing is watering down the term "engineer". If I had the time to go to college to get a legitimate degree, so can all other engineers — and I came from a poor family.

E.T.M.
Daytona Beach, FL

Dear Editor:

For once, I agree with Feerst.

T.G.
Holloman AFB, NM

Dear Editor:

Does the AMA or ABA allow open universities? I think not.

T.A.F.
Schaumburg, IL

Dear Editor:

Whole heartily and enthusiastically, I support Mr. Feerst in opposing non-accredited "schools" such as AIOU. A "degree" from this fake university is an insult to the education process.

The engineering profession has been hurt more than any other segment of today's society. Our professional societies, led by co-operating executives and college deans, has aided in this hurt. We desperately need men like Irwin Feerst to elevate the profession to its just position.

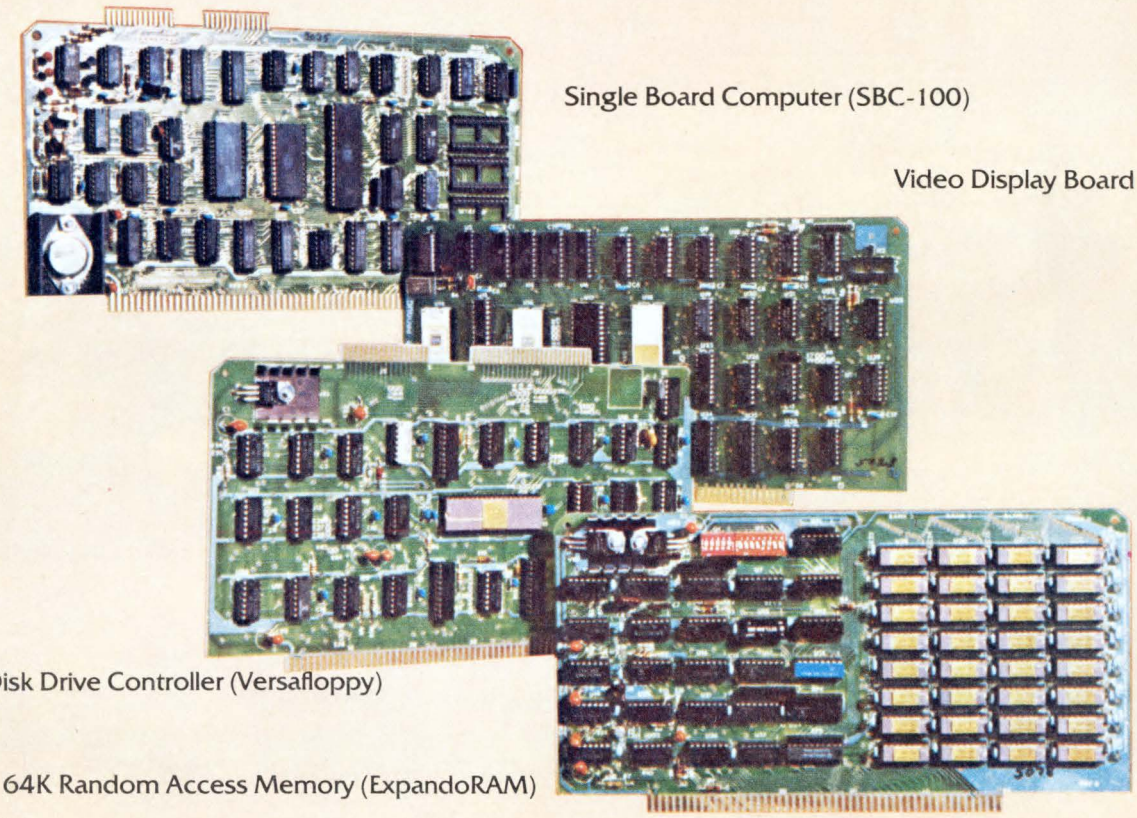
W.C.D.
Columbus, OH

Continued on p. 126

Guaranteed Compatible!

S-100 Bus OEM Boards

From SD Systems at reasonable prices



Single Board Computer (SBC-100)

Video Display Board (VDB-8024)

Flexible Disk Drive Controller (Versafloppy)

64K Random Access Memory (ExpandoRAM)

ASSEMBLED TESTED AND FULLY BURNED IN

The search is over for the convenience of S-100 Bus Computer boards that are really compatible and dependable. State-of-the-Art engineering, outstanding flexibility, rapid delivery, and low costs make the SD Systems computer boards the best OEM buy. The **SBC-100 Single Board Computer** is based on the Z80 microprocessor. Up to 8K of 2716 PROM, Serial RS-232 Port, Parallel Input/Output Ports, Software programmable baud rate generator, Four channel counter/timer, and 1K of RAM, all on-board. **VDB-8024 Video Display Board** features an on-board Z80 microprocessor for maximum flexibility in video control. 80 characters by 24 lines, displayed with high resolution on a 7×10 dot matrix. On-board Keyboard power and interface, 2K memory and a glich-free display by use of I/O mapped interface make this board the most superior board on the market.

The **ExpandoRAM** is available in 16, 32, 48, or 64K versions using 4116 RAMS. The population can be increased in the field at a future point if requirements change. Featuring Switch selectable boundaries, Bank Selectable Write Protect and using less than 5 watts, the ExpandoRAM is more reliable memory for the money than any other OEM board. **Versafloppy, Flexible Disk Drive Controller** with IBM 3740 soft sectored format compatibility controls up to four single or double sided disk drives either mini or standard size. **Full Line Software** includes Editor, Z80 Assembler, Linker, C-Basic, Complete Business Packages, System Diagnostic and Control Software and Disk Operating System. **PROM Programming Software and Hardware** also available. Circle the reader service number for full Technical Data... or call toll free to our Customer Service Department: 800-527-3460.

SD SYSTEMS

POST OFFICE BOX 28810 — DALLAS, TEXAS 75228

800-527-3460 — 214-271-4667 — TELEX 73-0151

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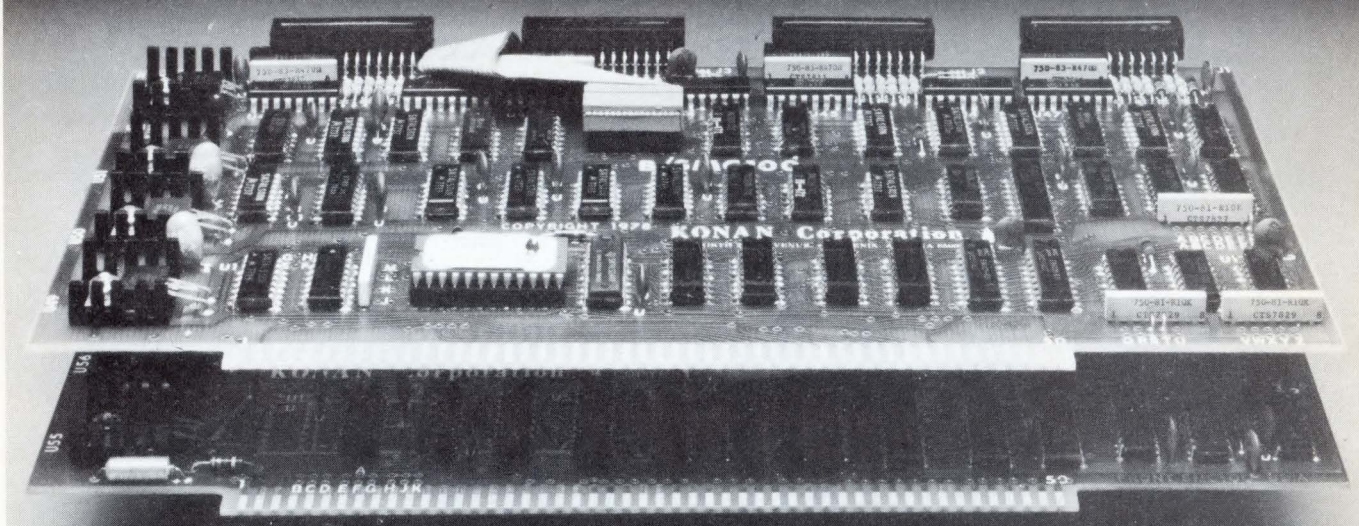
UP TO 1200 MEGABYTES OF HARD DISK CONTROL FOR THE S-100 BUS



It's versatile. It's fast. It's cost efficient.

It's Konan's SMC-100. The disk controller that brings S-100 bus micro computers together with large capacity hard disk drive.

Versatile.
It'll interface S-100 bus micro computers with all fixed or removable media disk drives with storage module (SMD) interfaces. These drives range from 10 to 300 megabytes per drive, including most "Winchester" type drives. Each Konan SMC-100 will control up to 4 drives . . . that's up to 1200 megabytes of hard disk per controller. And the SMC-100 let's you take your pick of hard disk drives (Control Data, Fujitsu, Microdata, Kennedy, Memorex, Ampex, and Calcomp, for example).

The SMC-100 works with your micro computer. It'll wait for your memory — it allows intermixing of slow and fast memories. It uses standard I/O instructions. And the optional driver ROM, addressed through descriptors, allows the SMC-100 to handle all disk interfacing, including error recovery and bad track mapping.

Fast.
The SMC-100 transfers data at high speed, 6 to 10 megahertz rates, with full on-board sector buffering and sector interleaving. Its DMA is considerably faster than most other S-100 DMA controllers.

Cost efficient.
The SMC-100 takes advantage of low cost-per-megabyte disk drive technology making the typical cost per megabyte about $100.

And the price is right.
The SMC-100 is a fast, efficient and versatile hard disk controller. It allows you to use low cost-per-megabyte technology. And, it's priced to keep your micro computer system micro-priced.

The O.E.M. single quantity price is only $1650, with driver ROM option. And excellent quantity discounts — and complete subsystems — are available.

Dave Baughman has the answers. Talk to him today. You can call him on Konan's order number: 602-269-2649. Or write him at Konan Corporation, 1434 N. 27th Avenue, Phoenix, Arizona, 85009.

KONAN

1434 N. 27th Avenue • Phoenix, Arizona 85009 • 602-269-2649

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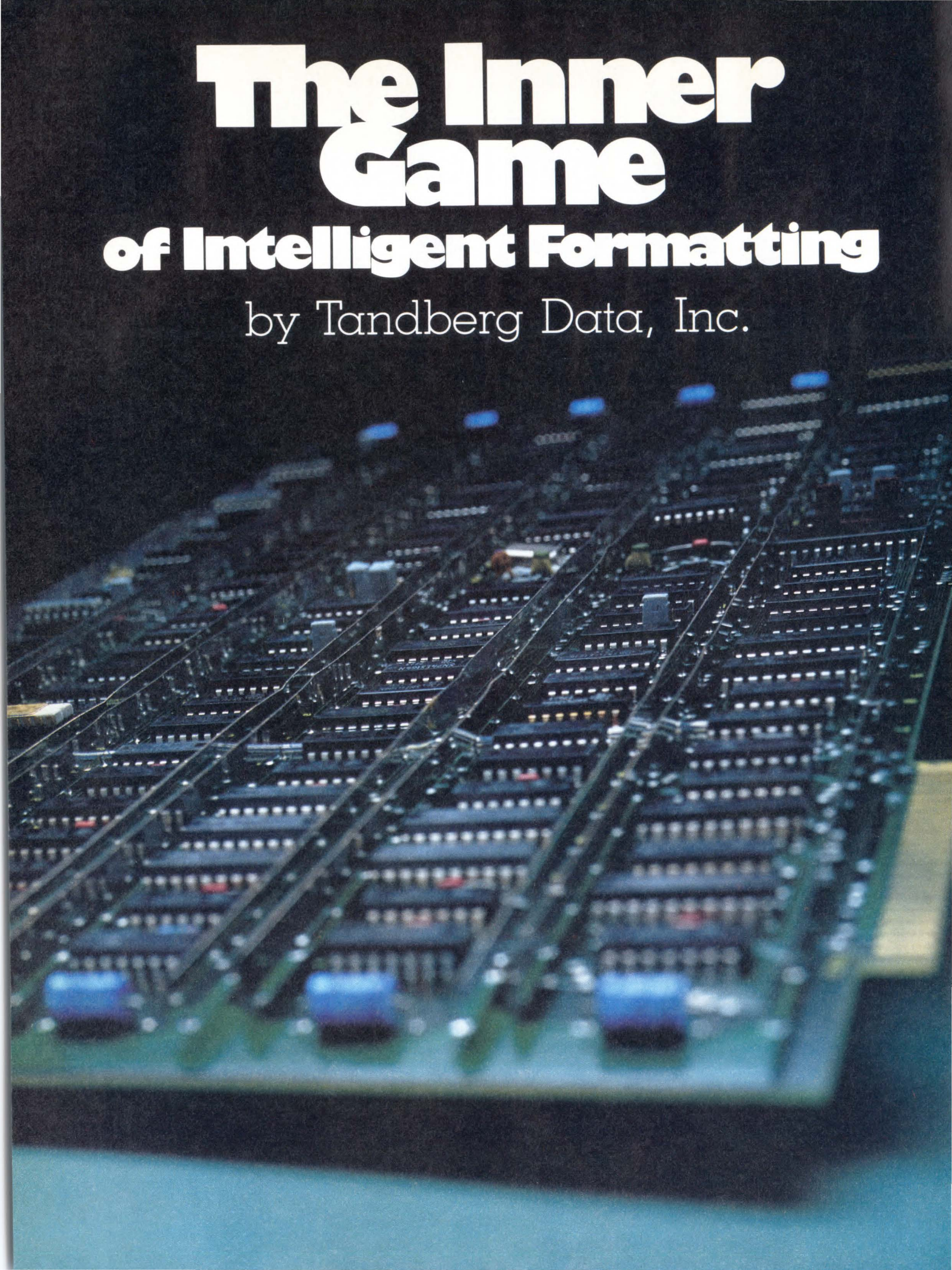
The Quietype.™

Now in OEM quantities. Ten years in development. More than a year of demanding field tests by OEMs. That's the Quietype heritage. The result: a reliable easy-to-use ink-jet printer that operates at 180 cps. Silently. Quietype's simplicity has made ink-jet technology practical for a host of applications. Now you can get quick delivery of full-featured printers or mechanisms—in OEM quantities—at sizeable discounts. Call Ed Zschau, our president, for a demonstration. Or write him today. He'll prove that silence is golden. Silonics, 525 Oakmead Parkway, Sunnyvale, CA 94086. (408) 732-1650.

SILONICS
Subsidiary of System Industries

The Inner Game of Intelligent Formatting

by Tandberg Data, Inc.



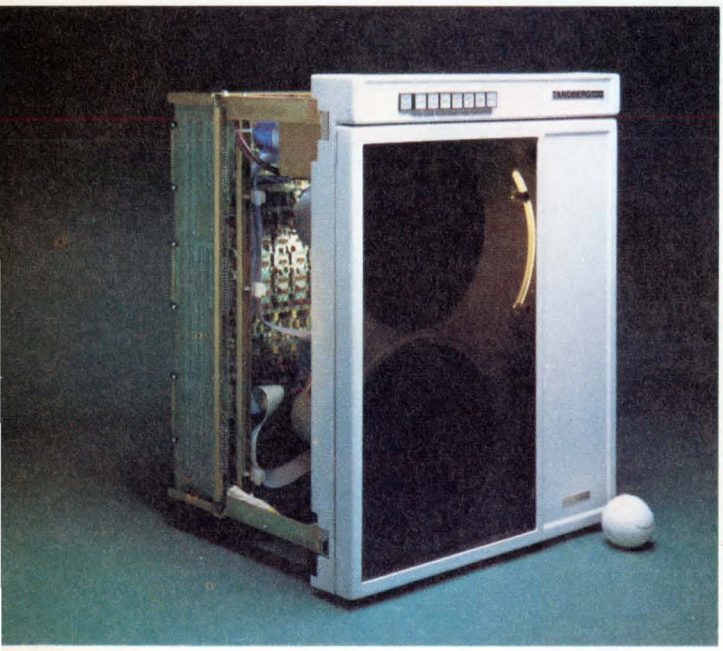
Get it together . . . and everything comes easier.

Put tape transport intelligence on the inside, and watch your game improve. It's possible with Tandberg Data's TDF 4050 (microprocessor-based) Formatter — now installed *internally* in the industry-proven, dual-format TDI 1050 Synchronous Tape Transport.

No more need for an external formatter to control the reading and writing of data. The interfacing task is naturally a whole lot simpler. And real savings follow with only one system to ship, handle, and mount, rather than two. Cost of ownership is resultantly the lowest currently obtainable.

The internal TDF 4050 Formatter reads and writes ANSI, IBM, and ECMA compatible tapes. It is designed to work with 9-track 1600 bpi PE and 800 bpi NRZI tape drives and 7-track 200/556/800 bpi NRZI tape drives.

Contained on one 19″ x 10″ PC board, the new Tandberg dual formatter can control from one to



four tape transports — either the same or half speed or a mix of different formats with dual stack heads.

The TDF 4050 can handle six different tape drive speeds. It can read and write PE and NRZI at the specified speed or one-half that speed when drives of different speeds are connected.

The TDF 4050 executes all standard commands, as well as other customer-specified commands.

Tandberg's TDI 1050 dual-format Synchronous Tape Transport utilizes 10½-inch reels. With the TDF 4050 Formatter, users may easily daisy-chain up to four transports simultaneously,

WHAT CAN THE INNER GAME OF FORMATTING DO FOR MY GAME?

1. Simplify interfacing.
2. Reduce integration time.
3. Eliminate redesign.
4. Facilitate daisy-chaining.
5. Cut shipping and handling costs.
6. Cut rack space and costs.

thus saving rack space and cost by freeing slots formerly occupied by an external formatter.

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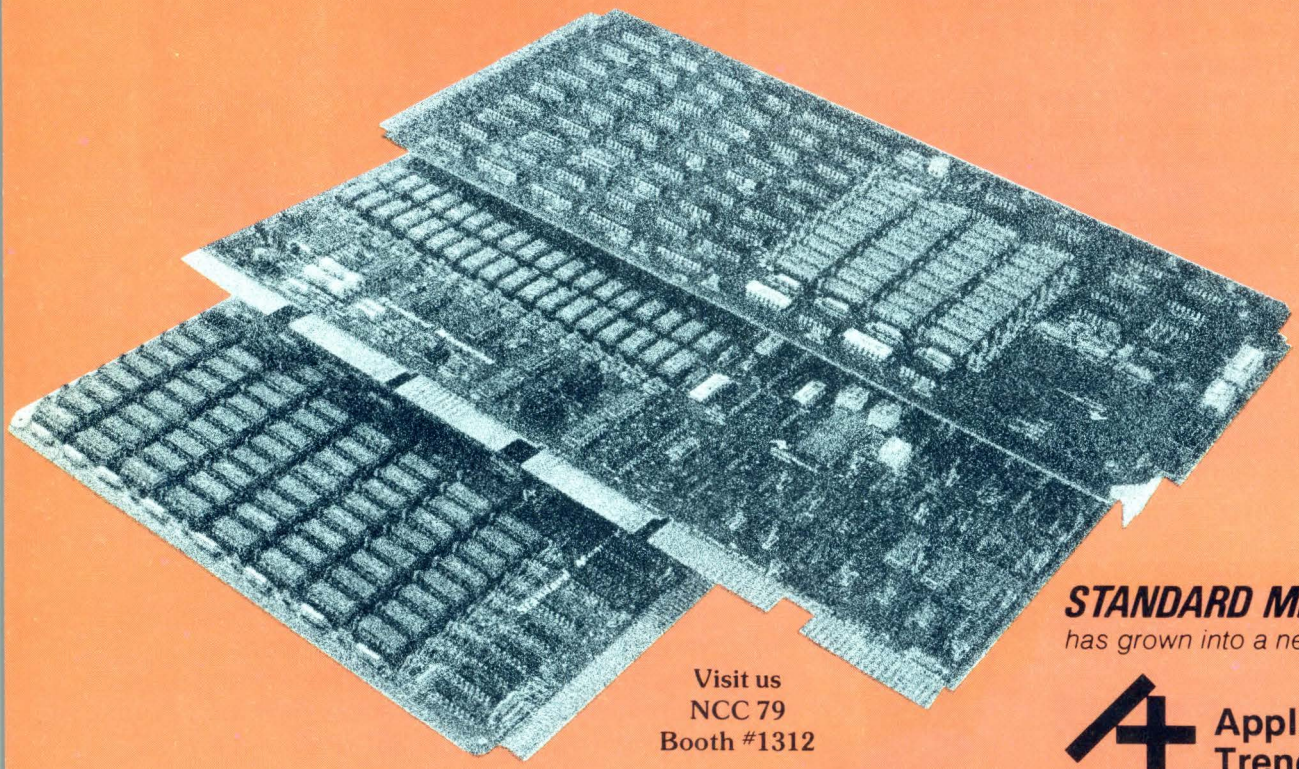

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TECHNOLOGY TRENDS

Vision One/20 Offers Digital Image Processing Improvements

This article describes the architecture and design philosophy of the COMTAL Vision One/20 Digital Image Processing System.

Theory of Operation

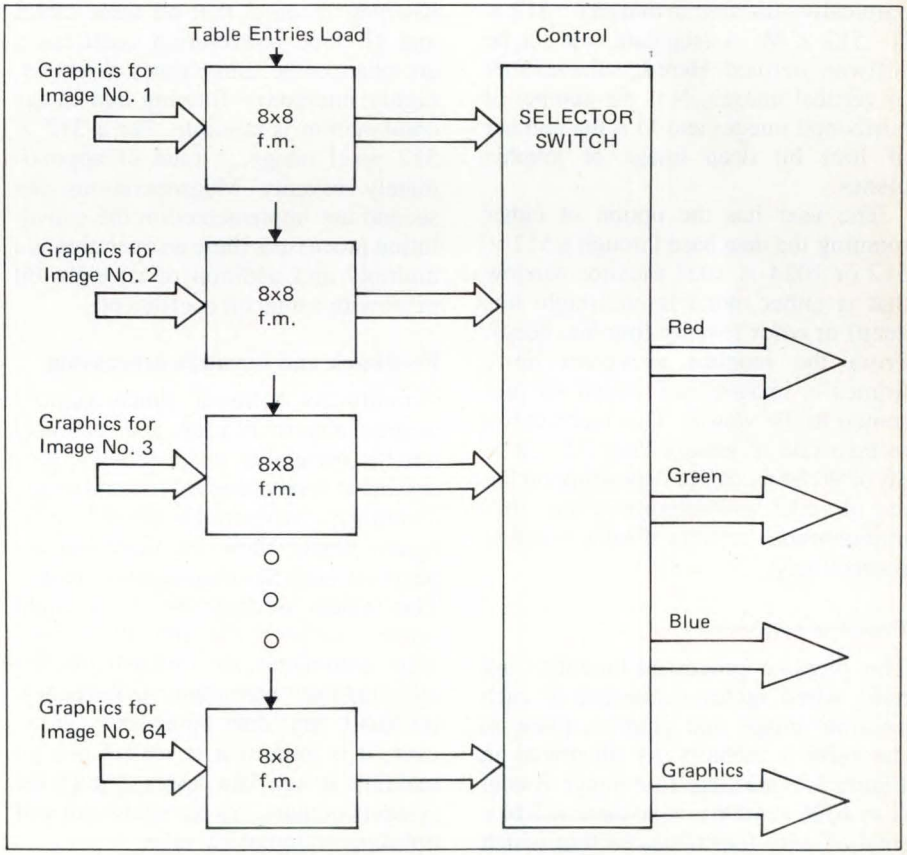
The Vision One/20 is a dual ported RAM refresh memory system which affords multiple user access to a common expandable data base (4096 × 4096 × 8 bit pixel memory images are available) with dynamic partitioning to afford a multiplicity of different applications. Real-time roaming with a window size of up to 1024 × 1024 pixels through the data base is possible with zooming and 3 × 3 convolution all implementable in 1/30 second. With graphics overlay memories; annotation, labeling, outlining and arbitrarily shaped multiple small area monochrome or color correction are possible. Due to the dynamic allocation of the data base memory, digital loop movies in real-time are possible as is left-right, right-left, up-down or down-up scrolling of new imagery into the refresh memory and viewing window. These and other features are expanded upon herein. Pipeline processors, freeze frame iterative image array feedback, firmware-burned control and instruction commands are descriptive of modern image processing architectures used in the Vision One/20.

Currently, the state of the art of digital refresh black and white as well as color displays seem to be hovering between 512 × 512 × 8 (×3 for color) and 1024 × 1024 × 8 (×3 for color) bits presented to the viewer 30 frames per second. It appears that constraints due to flicker and horizontal amplifier bandwidths will probably not provide significant breakthroughs above such resolution in the near future. Yet high speed RAM memories and clever architectures in the vision One/20 now allow the user to roam and zoom within far higher resolution digital images at TV refresh rates thereby permitting potential exploitation of a tremendous amount of data in "real time." (Here "real time" refers to the rate at which a human would want to change his scene of observation, it not being expected that he would wish to change it at a rate greater than 30 times/sec.)

Probably the most significant single aspect of the Vision One/20 is that of new architecture designs. The multiplexing of data channels, the pipelining of processors, the availability of high speed RAM refresh memory chips, the perfection of very high resolution color shadow mask and monochrome monitors all have combined to allow the development of this highly interactive image processing exploitation station. With RAM refresh, it now becomes possible to roam around a larger data base memory at will, as well as scrolling, and zooming in a simultaneous interactive environment. Again coupled with table look up monochromes and pseudocolor function memories, as well as the ability to partition a large 8 bit deep monochrome memory into 1/3 the size 24 bit deep true color memory, one obtains a truly interactive "digital light table" exploitation system. In addition to the breakthroughs provided by larger, cheaper, and random access memories, pipeline processing technology has also contributed to modern day image processing stations. Typical 3 × 3 arbitrary convolution filters followed by both linear and nonlinear function memory combinations can process a 512 × 512 × 8 monochrome image in 1/30 of a second (equivalent to a TV time frame).

RAM refresh memories

The refresh memory is comprised of 512 × 512 × 1 bit planes cycling at 800



MultiImage Pipeline Processors: 64 image input ports, 3 image & 1 graphics output port per user station, image port is 8 bits deep... 256 brightness shades, graphics port is 4 bits deep... 16 graphics colors.

nanoseconds per bit or spatial position. Four such planes are packaged on a card four deep providing one million bits of 16K RAM or one half of an image plane. A full 512 × 512 × 8 monochrome image requires two cards. Such a configuration defines an image plane, sixty-four of which represent a 4096 × 4096 image in refresh at one time. The architecture is configured so that each bit plane can be interpreted as a raster graphics plane; and in addition, the readout addressing can be configured so that image planes can be "stacked" to represent true color (three image planes or six cards), monochrome with four graphics (one and one-half image planes or three cards), or true color with four graphics (three and one-half image planes or seven cards). This configuration is represented in figure 1c. Because all bit planes are in synchronization, it is possible to offset the (x, y) starting location thereby providing arbitrary "roaming" capability. For a 4096 × 4096 image base a total of sixty-four separate 512 image planes would be roamable with no visual artifacting at the seams. In general, the memory configuration can be dynamically allocated so that an L · 512 × N · 512 × M · 4 deep data base can be software defined. Here L is the number of vertical images, N is the number of horizontal images and M is the number of four bit deep image or graphic planes.

The user has the option of either roaming the data base through a 512 × 512 or 1024 × 1024 monitor window that is either monochrome (eight bits deep) or color (twenty-four bits deep). From the monitor viewpoint thirty frames of imagery per second are presented to the viewer. This represents a refresh rate of greater than 7.5, 22.5, 30 or 90 M bytes/sec depending on the use of a 512 monochrome, color, 102 monochrome or color display window respectively.

Pipeline processors

The pipeline processor functions are hard wired tables connected to each possible image and graphics plane in the refresh memory as illustrated in Figure 3. For a sixty-four image system (i.e. 4096 × 4096 pixels) there will be a total of sixty-four tables each of which is an eight bit by eight bit (256 level by 256 level) function memory which can be loaded with arbitrary values under interactive operator control. These tables are loaded during horizontal and vertical retrace periods thereby guaranteeing no visual break up of the displayed imagery.

Convolution and image combination

Because all processing must be implemented at digital television rates, real time arithmetic operations must be developed extremely efficiently. For spatial filtering, small convolution kernels are fairly efficient and with iterative feedback, the effective domain of the kernel will grow. The convolution and image combination circuitry has been organized for maximum throughput speeds. Table look up techniques are used wherever possible and arbitrary entries in the tables are loadable at the users option. Quite powerful functions are implementable by this hardware configuration. Nonlinear entries in the function memory tables will allow spatially adaptive filtering, an example of which is low pass filtering in the dark regions and high pass filtering in the bright regions. Unsharp masking and other edge enhancement operators are all available with this architecture. Keeping in mind that all three tables and all nine convolution coefficients are changeable thirty times a second, highly interactive filtering and image combination is possible. For a 512 × 512 pixel image, a total of approximately seventy Megaoperations per second are implemented in the convolution processors (here an operation is a multiply and addition of an eight bit pixel with a nine bit coefficient).

Feedback and iterative processing

A multi-user station in which memory is accessible to all users and each user has his respective set of pipeline processors as well as convolvers and image combiners. An overall system block diagram would show the dominant aspects of such an exploitation station. The system is controlled by a small system computer through which firmware commands are initiated thereby allowing user interaction via keyboard, trackball, and data tablet entry. However, it is important to realize that no real time image data passes through the system computer, as its bandwidth will not support digital TV rates.

Probably the most significant aspect of the total systems configuration in a mathematical sense is the feedback path that allows the actual viewed imagery to be read back into memory in 1/30 of a second. This feedback permits iterative processing with pipeline processor tables, convolution kernels, and image combination circuits all updateable 30 times/sec.

Firmware control

Probably the second most significant breakthrough in systems configuration lies in the turn key operation provided by firmware (ROM) operating systems. One does not want the user to be an expert in digital technology as well as a software freak to be a productive user of such systems. Typically, the control of the architecture and data paths for the flow of such imagery are under control of a μP in which speed of transfer and control is the underlying objective. Responsive interactivity is the bottom line and firmware implementation at the front end exploitation station seems to be the current solution. The system computer with hardware arithmetic function in its own right, is an integral aspect of the system with all display processing hardware instructions stacked and processed via direct memory access thereby eliminating the normally encountered time-consuming operation of instruction I/O. The unique operating system includes over 100 high level language graphics and image manipulation instructions burned into firmware. Instruction programming, linking (MACRO's) and execution in software are all keyboard implementable. Firmware memory management by the system computer facilitates the handling of high resolution color graphic art imagery on the one hand, multiple station monochrome reconnaissance imagery on the other, and on to multi-level raster color graphics for a third application. Such memory management also lets the service engineer remove boards for repair or add blocks of memory. The system automatically senses which boards are connected online and makes best use of them. This dynamic allocation of memory truly makes the system a versatile image processing station.

Overlay control

The final card necessary to present the viewer with pictorial results of his interactive requests is the overlay card. This device has numerous functions, the most important of which fall into

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three categories: a) cursor/target definition, b) pseudo color implementation, and c) final display priority commands.

Because the Vision One/20 has the ability to present a 16 × 16 programmable cursor or target, the firmware commands selecting the target coefficients are implemented here. Each of the 256 (16 × 16) pixels defining the target has the ability of taking on eight different colors if so desired. Therefore crosses, circles etc. (i.e. all shapes and colors definable in a 16 × 16 array) are developed here. In addition, target position is developed here on an interactive basis for hand eye coordination updatable at a 30 times/sec rate.

A final set of 8 × 8 bit function memories are available for table look up prior to passing the image data on to the display. These function memories can be used for final monitor gamma correction or they can be used for generation of 24 bits of pseudocolor. In this mode of operation, the pipeline processor card causes one image to be placed on all three red, green and blue digital channels. Then each of the red, green and blue function memories can be loaded arbitrarily with 256 different values each to define any of 2^{24} possible color outputs. This capability now allows for the most subtle of detail to be made viewable by proper loading of these tables. Again, all coefficients can be updated 30 times/sec.

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Gray Scale Printer: Mechanics of Printing

The electric writing head assembly (Fig 1) is composed of eight stylus modules, in line, across the recording paper. Each module consists of sixteen styli, on 2mm centers, attached to beryllium copper leaf springs (Fig 2). A spring mount and drive rod system, called the "wag" assembly, moves the entire writing head in the direction of the line of styli to a displacement of 2mm. An optical encoder senses 16 equidistant positions at 0.005 inch or 1/8mm spacing as addressable picture element locations during this 2mm "wag" movement. These positions are sensed in both the left-to-right and the right-to-left scan directions. The encoder supplies direction and location status information to the data controller so that the proper time duration TTL pulse can be supplied to each stylus driver. Upon receipt of a TTL pulse, an electric arc of −160 V dc travels from each stylus through the carbon impregnated paper and to the grounded backup roller. In its travel, the arc burns a precise amount of coating from the paper surface revealing the carbon black base color. A pulse duration of 215μsec defines the 15th scale level, or black. Lesser amounts of time produce smaller burn areas, thus, lighter shades of gray. Sixteen (16) distinct levels of gray are possible in this system. Thus, the overall picture is produced by 16 × 8 = 128 styli × 16 positions each = 2048 picture elements over the 10.1 inches printing width. Each picture element has its own 16 level gray scale assigned when printed. Between wag directions and after each picture line is printed, the paper is incremented forward by a distance of 0.005 inch (1/8mm). The overall pic-

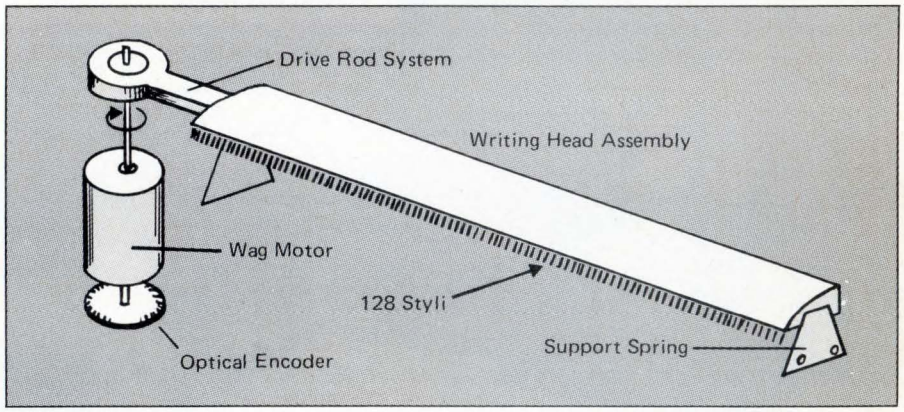

Fig. 1 CEC 912N writing head & wag system

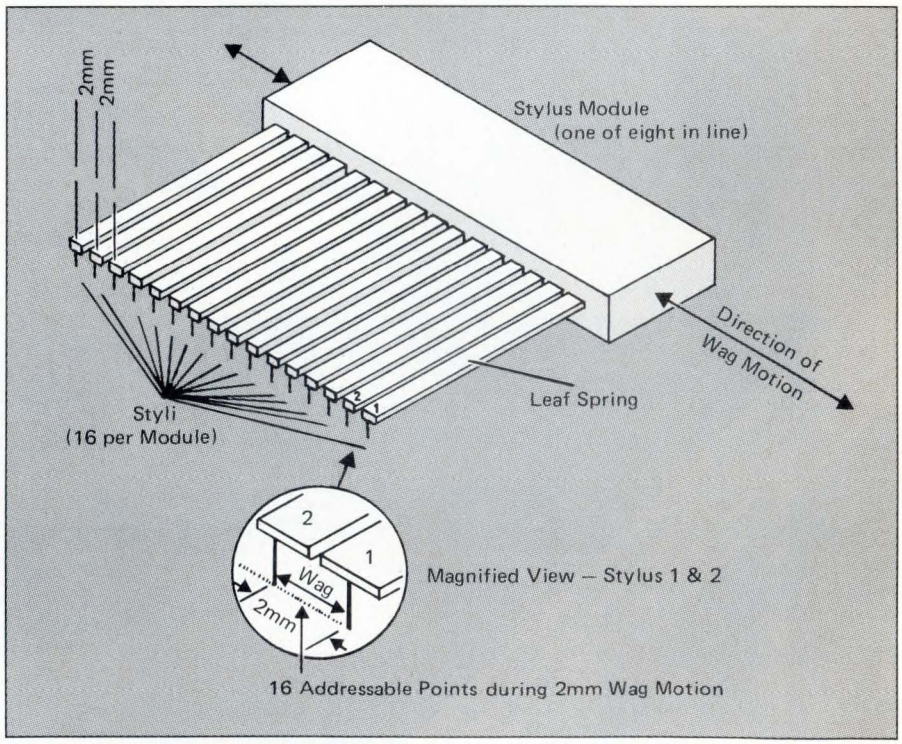

Fig. 2 CEC 912N stylus description

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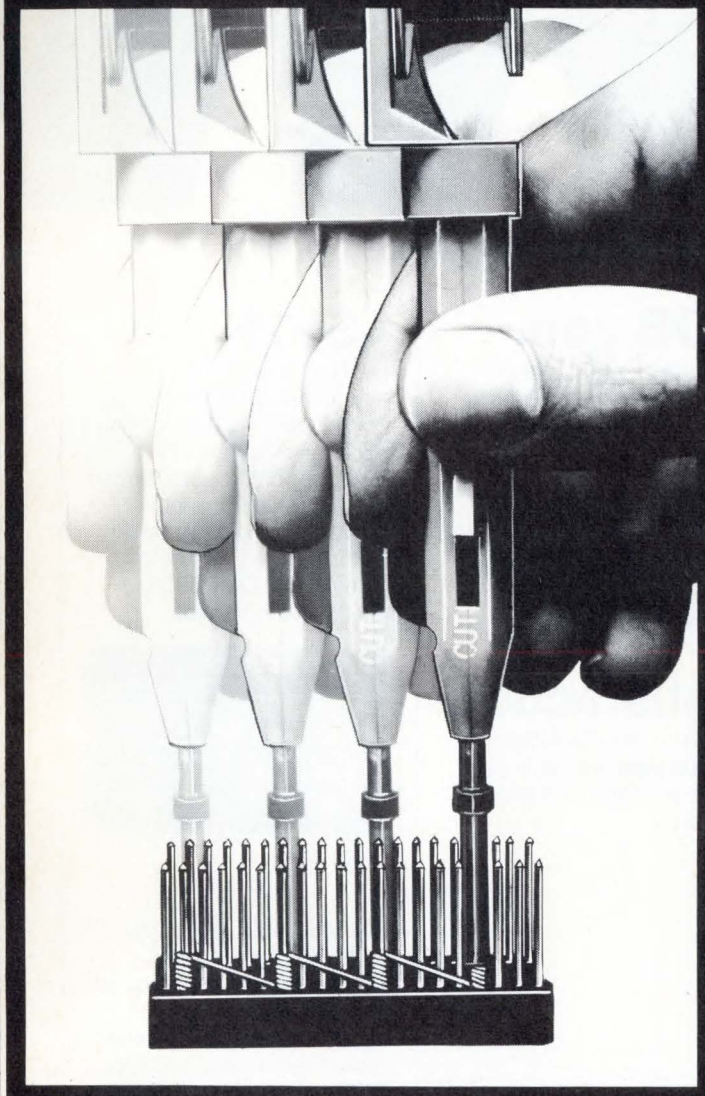

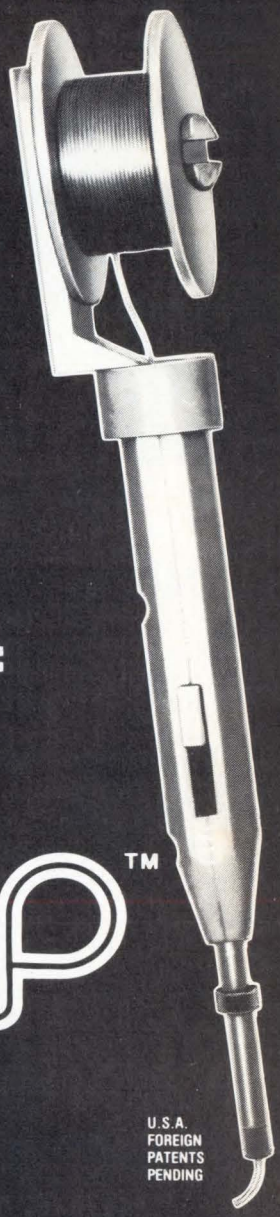

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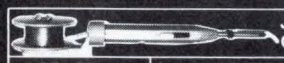 JUST WRAP TOOL WITH ONE 50 FT. ROLL OF WIRE		
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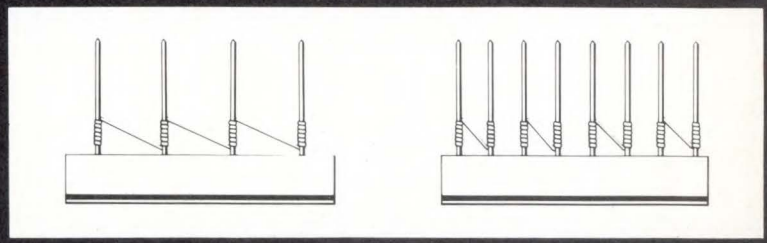

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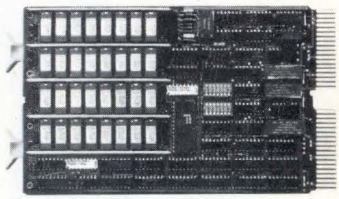

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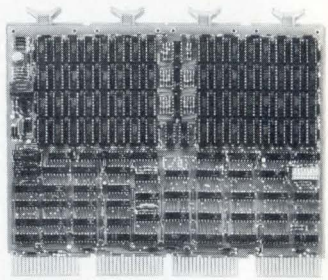

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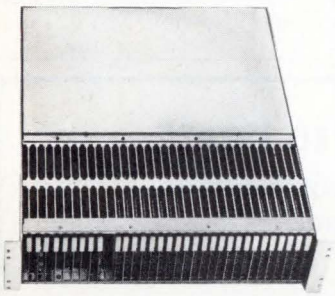

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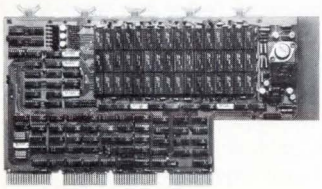

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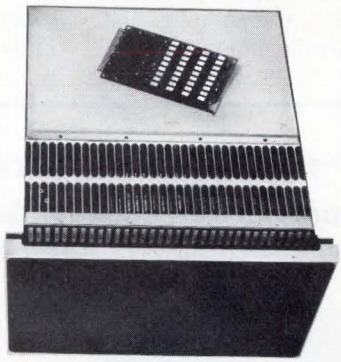

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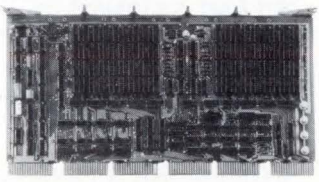

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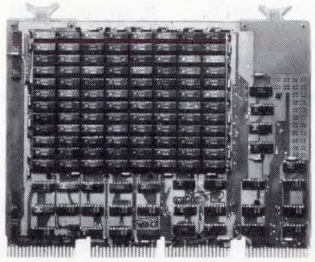

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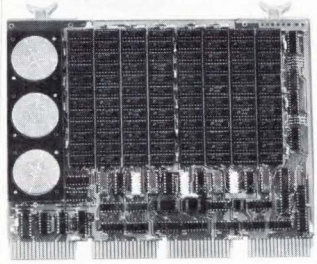

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INPUT DATA INFORMATION

Picture or graphic data is digitized into 4 binary words as defined by a gray level scale of 0 to 15 for each picture element (pixel) in the original. A maximum of 2048 pixels may appear in a single line, or raster, covering the 10.1 inch printing width of the writing head assembly. This data is stored in memory, with data for pixels 1 to 16 poised for printing by stylus #1. Pixels 17 through 32 are stored for stylus #2. Similarly, 16 pixel groups are stored for each active stylus through #128. At the proper time, indicated by the printer status signals, pixel data is converted into time duration pulses and transmitted at TTL level via 128 parallel lines to the stylus drivers. Each pulse defines a specific gray level to be printed at each pixel location. During the return scan excursion of the head assembly, pixel order is reversed so that stylus #1 prints pixel 16 first, then down through the order sequence to pixel 1.

μP-Based Systems Testing Seminar

Testing μP-based systems is a hot topic, yet few experts exist; and those who are proficient command high salaries. Interested in testing μP-based systems? Polytechnic Institute of New York and the Institute for Advanced Professional Studies will present a five-day intensive seminar for design and test engineers. The seminar, directed by Dr. Glen Marston, is titled "Testing Microprocessor-Based Systems," and prominent faculty will conduct guest lectures, demonstrations and provide assistance with work-related problems submitted by participants.

The seminar will be held June 11 through June 15, 1979, at The Colonial Hilton Inn, Wakefield, MA. The workshop enables participants to coordinate μP-based product design with production testing. Emphasis is placed on product design practices influencing testability, test equipment capabilities, limitations, and test programming and diagnostic software development.

The following topics are just some of those to be covered: μP architecture and programming, μC system configuration and support chips, design practices influencing testability, common faults in μC-based systems, troubleshooting during development (equipment, applications, capabilities, limitations), coordinating design with production test strategies, test programming and diagnostic software development, production testing equipment (capabilities, applications, limitations, test equipment for custom components), recurring and non-recurring costs, and reducing testing costs.

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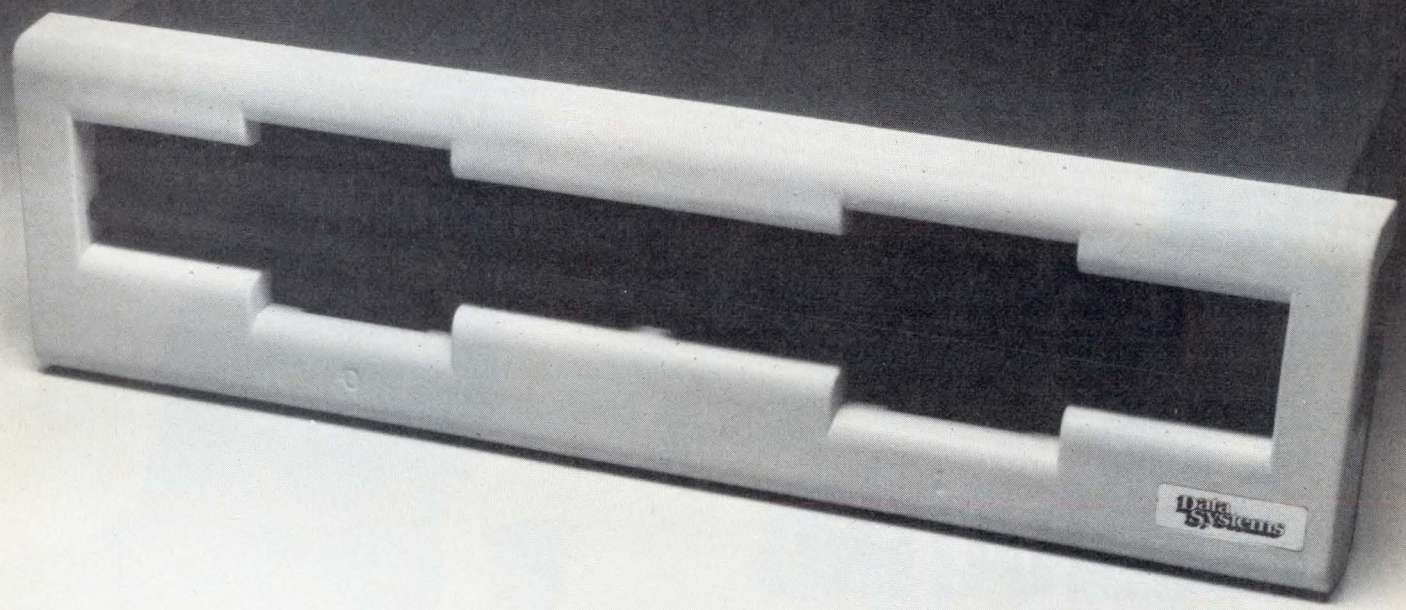

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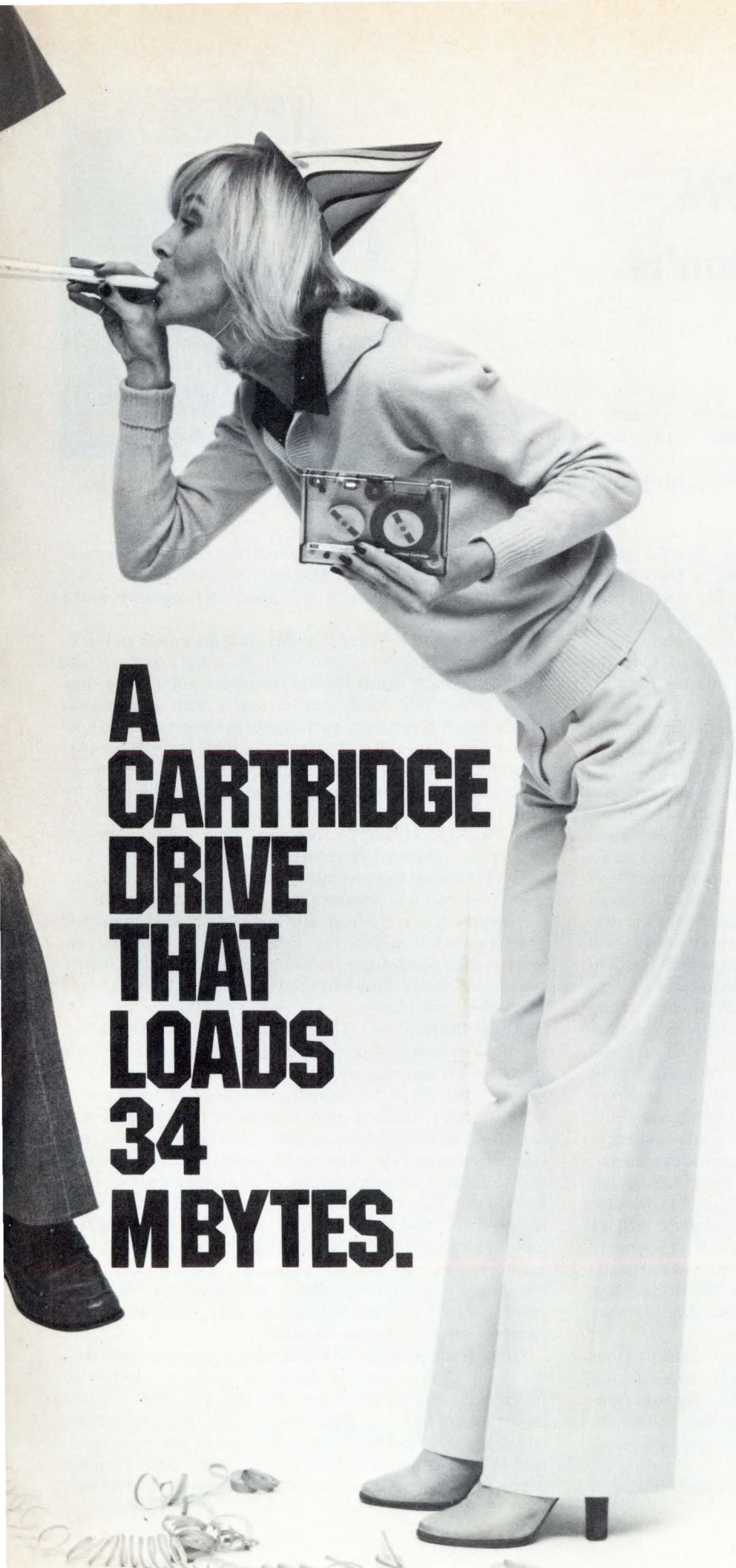

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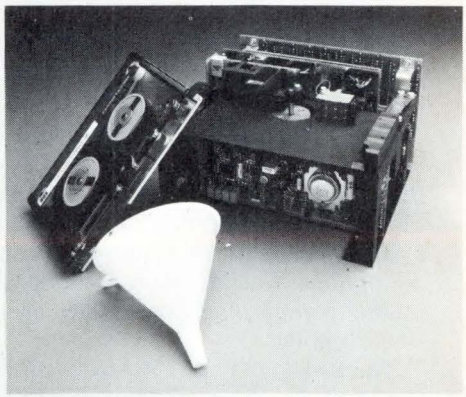

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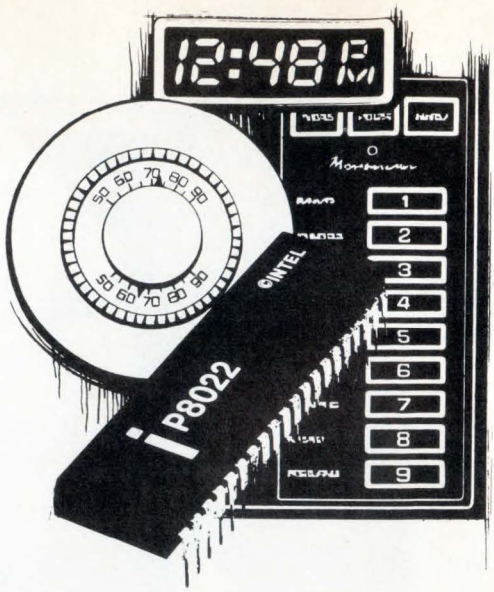
PART TWO

µP SELECTION
Some Do's and Don'ts



Paul Snigier, *Editor*

In the first half of this series, we warned that EEs who select a micro that's not commonly used could be gambling with their corporation's future. We compared 8- and 16-bit micros, single-chip micros and examined mid-range micros. We now will look at some 16-bit micros and then provide guidelines for selecting a micro.

Beyond the 8-bit µPs presently available lies the 16-bit micros, some available for some time (PACE, TMS-9900); others, like the 8086 and LSI-11/23, have only recently been announced; and still others, like the Z8000, MC68000 and others are just entering the scene or are coming soon.

Downgraded minis that are offered as 16-bit µCs provide architectural advantages over other 16-bit micros. The LSI-11, microflame (9440 and 9445), and TMS 9900, all minicomputer derivatives, are based on the designs of minis. Not surprisingly, these micros offer more powerful and easier-to-use facilities. For example, the 9900, if its 16-bit capabilities were removed, would still be sophisticated compared with present micros. Although the LSI-11 has gained some acceptance, it's too early to tell how the 16-bit microcomputer race will go. Also, new contestants, such as Rockwell's Super 65 and Fairchild's Microflame II (four times faster than the 9440 and ten times faster than Data General's Nova 3 mini), are expected to keep entering the market. For us to make a valid comparison between them at this moment is not possible. Therefore, we describe them in general as examples of what is presently available, or about to come.

Activity in the 16-bit arena is risk, with product family announcements arriving on our editorial desks every other day, it seems. As I write this (March 9), the latest 16-bit release to arrive is from DEC, announcing "the world's most powerful microcomputer — the LSI-11/23." This downgraded mini has the functionality and software compatibility of a midrange mini on two 5.2''-by-8.9'' boards and backplane and costs under $1800 (or $4500 for a rack-mountable, packaged version). Both run the RSX-11M and -11S operating systems available before now only on mid- to high-range PDP-11s. It runs all software developed for the LSI-11 family without modification, including the RT-11 operating system and high-level languages (Basic, Fortran IV, Focal). An optional floating-point processor chip, the first for any micro, permits five times faster operations than software floating point.

The LSI-11/23 has 256 kbytes of memory capacity (four times greater than the low-end LSI-11/2), uses the full instruction set of the PDP-11/34 and has the software-supported memory segmentation and protection features of the RSX-11M and -11S multitasking, multiuser operating systems.

DEC's entry runs two to five times faster (depending upon configuration) than their previous LSI-11 family members. Cycle time is 290 nsec (CPU) and 500 nsec (memory); add time (register-to-register), 1.7 µsec; and memory access time, 210 nsec.

Where would a system designer want the power and flexibility of such a super micro? Well, the small board size and high component density would permit designing more computer power into much smaller spaces than conventional single board computers, particularly in instrument and control system design. It will probably be designed into complex instrumentation, as central elements of special business-oriented systems. And since it's plug-compatible with the LSI-11/2, as well as software compatible with the LSI-11/2 and PDP-11, it already promises wide-ranging upward migration. Another interesting factor is how DEC offers its LSI-11s through independent computer dealers and can offer good customer and field support — both definite plusses.

Industry observers have felt that downgraded minis and true micros fall in different niches for many different reasons, so that competition isn't direct and comparisons hard to make. We wonder how long this will remain true, if it already hasn't begun to change.

Texas Instruments's TMS 9900, with its 16-bit registers, employs memory-to-memory architecture in which the focal point for the instructions is the memory rather than a set of on-chip registers. A single instruction can fetch two operands from memory, perform an arithmetic or logical operation, and store the result in the memory. This is possible because instruction execution steps (clock cycles) vary from instruction to instruction under control of an on-chip microinstruction ROM. Beyond this bold departue from conventional accumulator based architectures, the TMS 9900 employs eight addressing modes, five of which refer to a set of 16 memory words defined as "registers" in a workspace. By changing the contents of a single on-chip register (the workspace pointer) multiple workspaces may be defined or located to enhance program flexibility.

Other features of the 9900 that make it more powerful than the 8-bit devices are the hardware multiply and divide instructions and the bit-addressable I/O. The 9900 employs three types of I/O: 1) memory mapped I/O, in which memory addresses serve as I/O locations for input or output information to be sent over the data bus, 2) DMA (direct memory access) in which an external controller may suspend proces-

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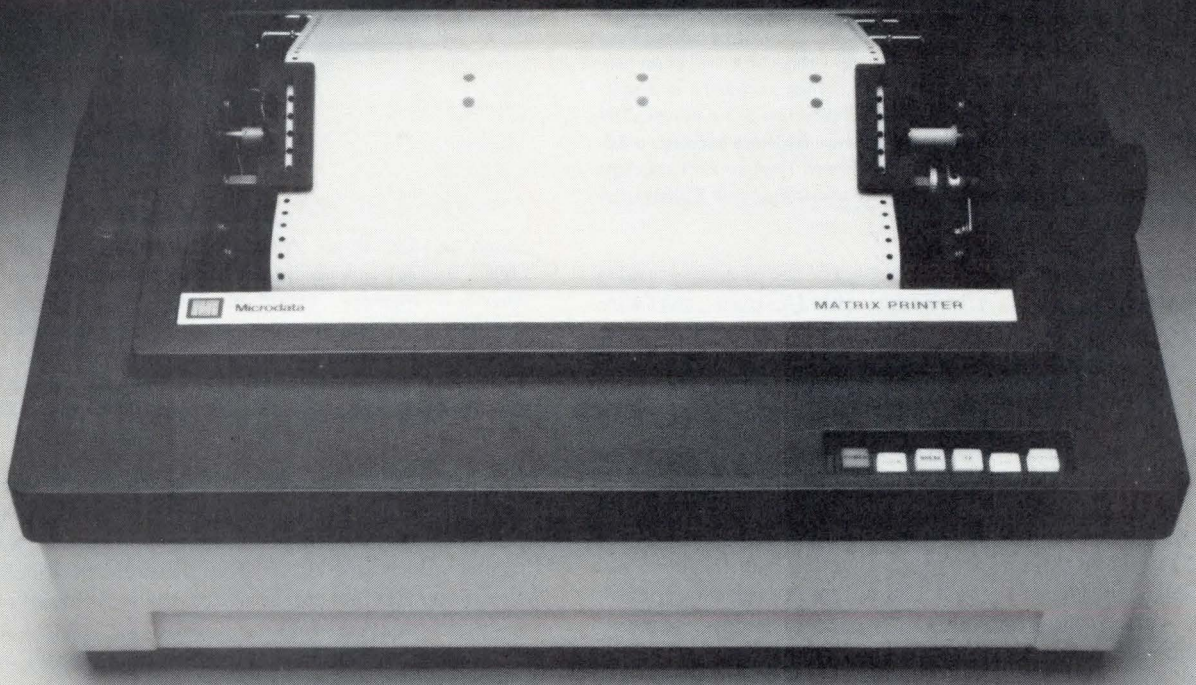

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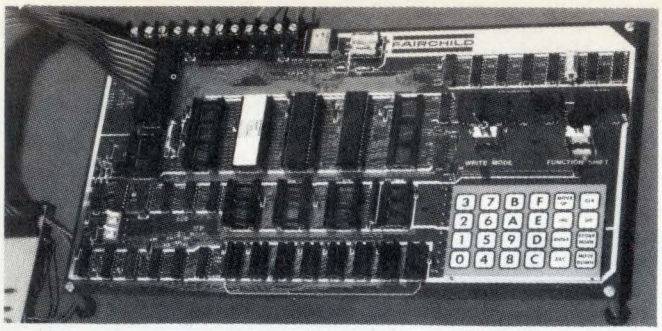
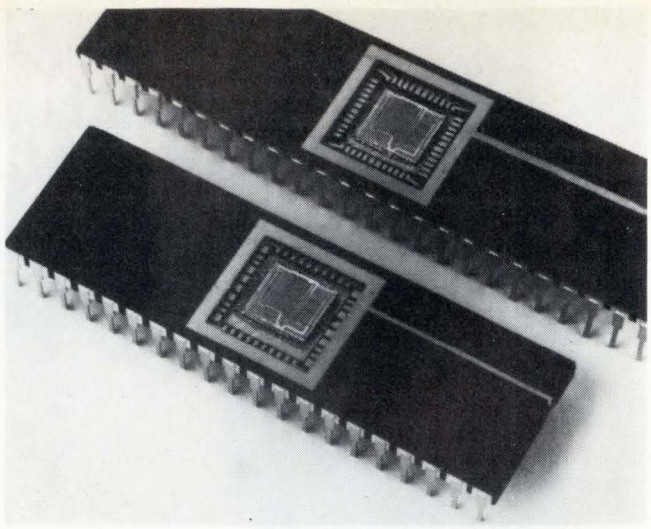


This user-board from Fairchild is typical of the improved support being offered. With this PEP (prototyping, evaluation and programming) μC users can write programs and debug hardware and software for F3870, 3872, 3876 and 3878 single-chip μC systems. The board provides real-time, in-circuit emulation of these through a 40-pin umbilical cable, and includes an on-board keypad and six-digit LED display, as well as sockets for programming the F38E70 or 2716 EPROMs.



Zilog's N/MOS 16-bit Z8000 comes in two versions: the 40-pin Z8002 (below) and the 48-pin Z8001 that allows users to address 8 Mbytes of memory. Z8000 possesses 24 on-chip 16-bit registers that reduce the number of memory references needed in programming. The instruction set supports 7 data types, has 8 addresssing modes and 418 usable opcode combinations. "Z-Bus"-compatible peripheral and memory devices will soon complete the Z8000 family.

sing while data is transferred between the memory and a peripheral device, and 3) bit-addressable I/O over a two-wire interface which works with the address bus. Up to 4096 single-bit devices may be addressed for inputs and another 4096 single-bit device may be addressed for output when information is to be transferred one bit at a time. Multiple bit transfers may also be made over the same interface because instructions are available for transferring any number of bits from one to sixteen to or from a peripheral device. This I/O feature makes the 9900 particularly useful in process control where single bit devices are used as well as multibit devices. A variety of devices may be accommodated even though they require various bit groups (e.g. 2, 4, 6, 8 or 10 bits) because the processor easily handles this data transfer type.

Why isn't the TSM 9900 as popular as the 8080A, for instance? On its bright side, TSM 9900 can transfer from 1 to 16-bits at a time; 8080A, only in 8-bit increments. The 9900 requires less instructions to transfer data into memory, than does the 8080A using its accumulator I/O method. Some pundits claim that the 9900's architecture, though more powerful, has hurt it; and system designers find the 8080A architecture easier to comprehend, and therefore, easier to use. On a similar vein, this is reflected by the popularity of μC kits for personal computing engineers: only until two months ago did we see a TI board available.

On an unrelated topic, since I^2L and NMOS 9900s are now available, this is a definite plus factor for TI's family. Offering a micro in various semiconductor technology versions, such as the RCA-Intel contract to manufacture CMOS 8048s, cannot but help add to the device's popularity, since a CMOS version opens up applications where low-power dissipation is a paramount design factor (e.g., in portable test instruments and other battery-powered equipment).

Aside from the mere difference in word size, 16-bit micros typically differ from 8-bit devices in architecture; the larger unit is made for higher data throughput as well as increased data processing type applications. However, many areas exist where both devices share common type architecture. The TMS 9900, like the 6800, uses a memory-to-memory configuration in its architecture to achieve multiple register files. Unlike the 6800, though, the 9900 designates the first 32 bytes of memory as workspace registers to replace what would typically be hardware registers.

Other features of the 9900 that make it more powerful than the 8-bit devices include hardware 16-bit multiply/divide capability, and direct, command-driven I/O capability. The multiply and divide operation typically require 15 and 37 μsec execution time, respectively. In its I/O operation, the 9900 more closely resembles the 8080 than the 6800. For I/O operation, the 9900 has 12 address lines and is capable of directly addressing up to 4096 different peripheral devices. Moreover, I/O bits can be addressed individually or in fields of 1 to 16 bits, thus making it useful for control applications which involve sampling the state of a switch or indicator (represented as one bit in an I/O word).

Available for some time now, the 9900 represents the previous generation N-MOS semiconductor technology. With the advent of the newest 8086 processor implemented in H-MOS, an order of magnitude increase in performance over the previous generation 8080 has been added. What accounts for processor performance ten times greater than previous 8-bit devices? It is the ability to address a full Mbyte of memory. This compares to a maximum of 64K for the 8-bit micros and the 9900. Such large addressing capability makes it easy to build very large systems around the device.

In addition to the expanded addressing capability, several addressing modes have also been added to the 8086, thus better suiting it for traditional data processing applications, base relative, indexed and relative. With these addressing modes, an address can be modified by a register, an index register, or the sum of both the base and index register. Additionally, an optional 8-bit or 16-bit displacement can be added to each of these register values. Thus, word addresses can be produced very flexibly while instruction size is kept to a minimum. Moreover, these extra modes make it very easy to dynamically relocate program code.

Like the 9900, the 8086 (second-sourced by Mostek) has hardware multiply/divide. Furthermore, like the 8080, the processor supports reentrant code. However, unlike either of these devices, the 8086 contains an elaborate string handling capability, a set of instructions specifically intended to handle alphanumeric strings. One of these instructions can, for example, move a block of 64K bytes from one portion of memory to another.

Other areas in which the 8086 has significant new capability is in I/O handling. Besides extending the I/O addressing range to 64K bytes of I/O port space, the processor permits

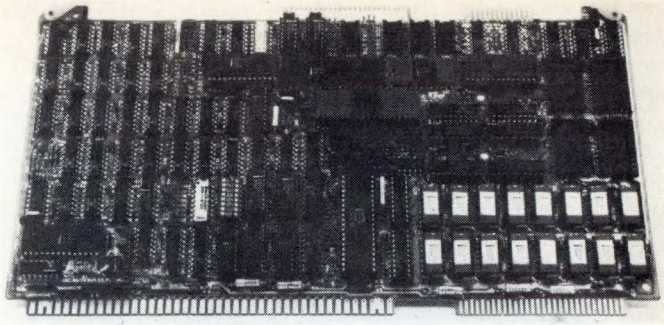
The 16-bit 4 MHz TMS990-40 is maximized by using separate address and data buses to avoid multiplexing delays. Three separate I/O techniques are supported, including DMA, and CRU (providing optimum control line manipulation without using memory space). The CRU provides a simple, single command page switching capability for memories larger than 65K bytes. The two address format of the TMS 9900 provides greater compaction for short operations like (P+Q), whereas the more popular one-address architecture excells at longer operations. Which is better? It depends on application, programming style, efficiency and frequency of long expressions.

memory mapped I/O addressing as well. This means that the new addressing modes used to access memory can likewise be used to access I/O ports. Beyond the expanded I/O capability, the 8086 also contains a vectored interrupt structure similar to the 8080 which consists of a memory table that permits the 8086 to service 256 different types of random interrupts.

Improvements in the architecture which have contributed to the performance of the 8086 include its elaborate register structure. In place of the seven registers of the 8080, the 8086 contains fourteen. Moreover, the manner in which instructions within the 8086 are executed have also been improved over methods used in the 8080. For example, in place of the sequential access of program instructions from memory, the 8086 uses a pipeline technique. This means that as one instruction is being executed the next instruction in the sequence is being accessed from memory. Since memory access typically can occur faster than some instructions can execute, it is conceivable to have several instructions in the program accessed and queued up ready for execution. This considerably reduces program execution time in most programs.

Going beyond the 8086 are the Z8000 and MC68000. Both have large register sets (16 registers or more) and expanded addressing ranges (8 Mbytes for the Z8000 and 16 for the MC68000) and include multiply and divide instructions and the ability to do high-level string operations. These modern μPs allow re-entrant and recursive programs, support high level languages efficiently and allow users to write position-independent code.

An unusual feature of the 68000 is its internal architecture: it has 17 32-bit registers, all its internal data paths are 32-bits as well as its ALU. The only feature of the machine that is 16-bits is its data bus. Some engineers might tend to regard the 68000 as a 32-bit μP — not a 16 bitter. This 32-bit internal architecture allows fast address computation to support direct addressing of the 16 Mbytes address space. The ability to do fast and extensive address computations is important for the efficient support of high-level languages (such as PASCAL and COBOL). The 68000 can use eight of



The iSBC 86/12, based on the 16-bit HMOS 8086, supports a 1 Mbyte address space and adds a new dimension to the realm of choices available in selecting the appropriate processing power.

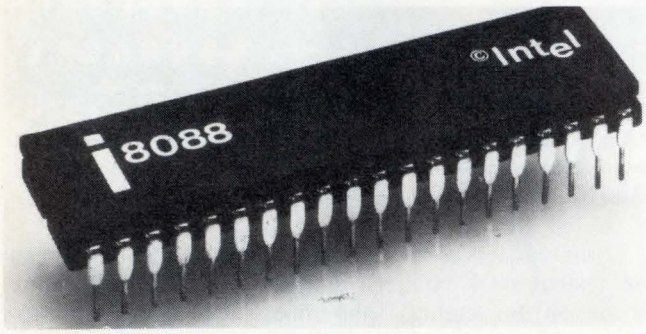
its 32-bit registers as stack pointers (7-user stack pointers and one system stack pointer), and with its Link and Unlink instruction for calling subroutines, and its memory-to-memory Move instructions utilizing post increment and predecrement modes of addressing, the 68000 can operate much like a stack machine (as well as the traditional Von Newmann machine). This allows for very efficient implementation of the kernals of a number of high level languages (including microFORTH and PASCAL). Z8000 is second-sourced by AMD. The center of the Z8000 family is the Z CPU, which possesses 16 16-bit general purpose registers, 8 user-selectable addressing modes, 7 main data types, and instruction set exceeding 110 distinct instructions. Two versions of the Z CPU exist — a 48-pin segmented version directly accessing 8 Mbytes/address and a 40-pin, non-segment version directly addressing 64 kbytes/address space. Now that we've looked at some of the more popular micros, let's see if we can help you decide which micro to select.

Why gamble?

System designers who select a micro that's unpopular are gambling, increasing the likelihood that their choice will be left unsupported — or provided declining support in the future.

Which micros will have a greater chance of surviving in the microcomputer jungle? We've discussed some of them. Leaders — 8080A, 6800 and Z80 and their variants — will be there, of course, as will be others. Many unpopular micros won't die — just age, with less and less support. Lock into one of these and you're in trouble. We won't mention some of these micros; you know them as well as we do. In case you're not sure about a micro's future, there is one clear factor that stands out above all others — a micro's popularity with designers. If users are scrambling to use a micro, you can bet that it will be around for some time and support (CPUs, memory, SBCs, etc) will be there. Still not sure? Check to see how popular the micro is with manufacturers, that is, the number and quality of alternate sources. And, it should occupy at least 10% of the market. If the alternate sources are numerous and large heavyweights, then their marketing departments have given that micro their vote of confidence. Conversely, if there is only one, smaller firm second-sourcing that micro, watch out. Then, too, don't neglect to see what exists in terms of development aids provided by the big semiconductor makers, whose marketing departments, once again, give their vote of confidence for supporting those micros that will survive the best. Of course, the supreme stamp of approval is the Department of Defense, which only accepts those micros (6800, 8080A, 2901A) that they anticipate will remain on the scene for a good while. In your search, do examine documentation and manuals for

lucidity and quality. If the firm isn't willing to put enough support into writing decent documentation, I'd seriously wonder if this reflected their marketing department's attitude — that they don't consider their micro a viable competitor. The days of poor micro documentation should be behind us at this point of time. We are reviewing some excellent preliminary microcomputer documentation from a major



Intel's new 8088 contains the 16-bit internal architecture of the 8086 combined with the 8-bit bus interface of the 8085A to give it performance surpassing other current 8-bit devices.

manufacturer; its clearness and quality rate it as excellent, and it is typical of the improved quality of microcomputer documentation now being put out by manufacturers. It's a rule-of-thumb, albeit a general one, that popular micros are supported by good documentation. Whether it's because poor documentation, manuals and sales literature turn off would-be users, or vice a versa (i.e., lack of users prevents sufficient funding for documentation), is a moot question. The effect is the same: poor documentation turns off users, many turn to competing micros, and a poorly-documented micro gets less and less popular. The next step is obvious: the competing micro that users turn to is then offered in a variety of forms (for example, single-board offerings, such as Intel's SBC 80 line). This in turn, creates a positive feedback effect, encouraging even greater use of that micro.

But beware: poor coverage of a micro in the electronics press or by book publishers is only a rule-of-thumb and not necessarily a true guide to a micro's popularity. Exceptions exist. Products manufactured in high volume, such as TV games, car radios or microwave ovens, will use micros where the overriding cost of the device and its supporting parts, not to mention production cost, are the main factor. Device sophistication, simplicity, good documentation and other factors all take a back seat to one factor — lower cost. But don't expect to find that much coverage in the trade press. Because they are mask programmed during fabrication, these devices only make sense from a custom order standpoint. They can only be used in high-volume products. Design and development will be extensive on high-volume run products; every nickel shaved from such a product is well worth the $5k in engineering design and development if volume exceeds 100k.

Ease of usage and education count

Consider the ease of usage. For example, the TMS 1000 series remains a popular 4-bit micro among designers and manufacturers because it is easy to program. Most programmers are not software geniuses, and the rapid evolution of micros simply has made it impossible for designers to acquire sufficient expertise to write elegant programs (which certainly is not the goal, anyways, since getting the product into production fast is the real objective).

The case of the TMS 1000 brings to mind the matter of

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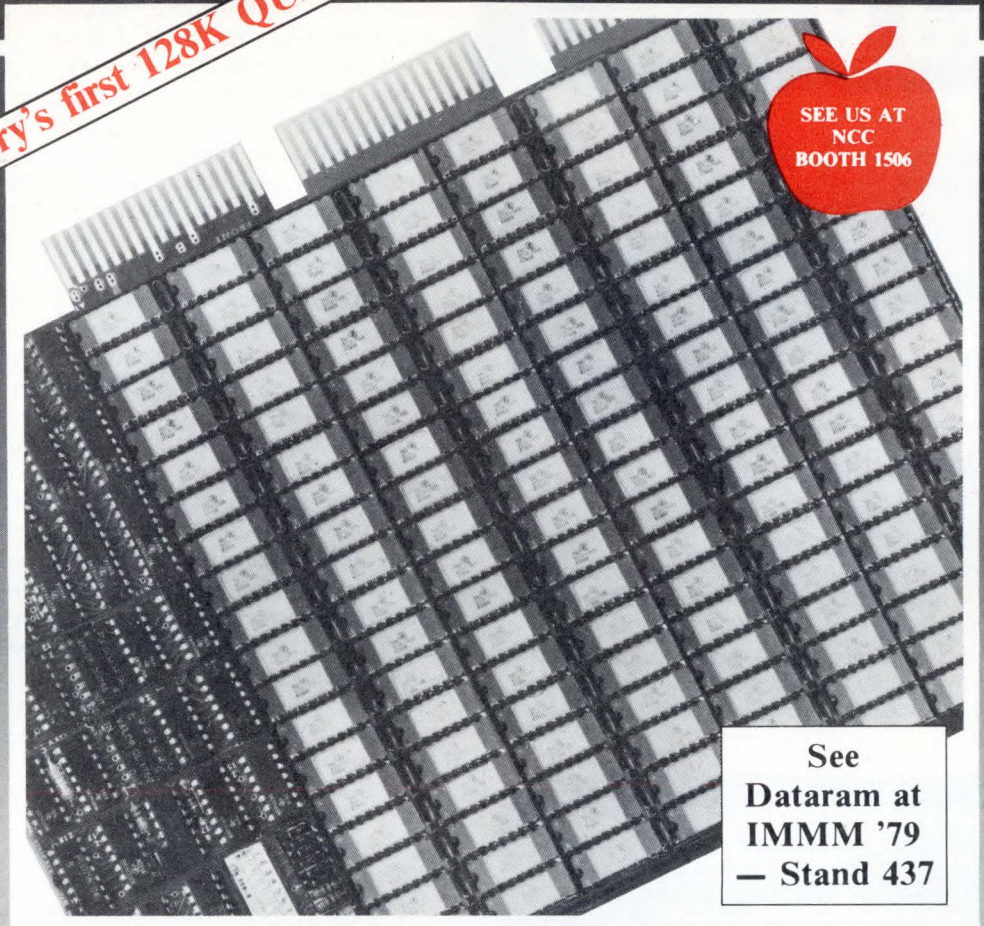

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education or training. Programmer-designers often prefer easy-to-understand devices. Naturally, the converse is also true. For example, the 16-bit, 64-pin TMS 9900 (NMOS) and its cousin the SBP9900 (I^2L), despite all their versatility, haven't become the most popular of micros. Viewed from an education vantage point, this isn't surprising, since no one has ever accused the TMS 9900 of being a simple micro to design with. This is not to deny other negative factors, such as the 9900's great flexibility being offset by the necessity for add-on devices that increase components count and layout complexity, and decreased reliability from greater interconnections (not to mention higher assembly and testing costs). Small wonder that some users opt for less-optimized-but-expandable single-chip micros.

This is not said to minimize the 9900's many advantages. By selecting appropriate auxiliary devices, the 9900 is configurable to many applications. It's interfaceable to customized TTL units, provides *true* software compatibility (which is rare) and has all-external memory, thus providing it with flexible memory size. These advantages combine to make it very well-suited to a wide spectrum of system-building possibilities. I use these examples to show that: 1) no one or two micros are suitable for all applications and that 2) you must examine all tradeoffs for your intended applications.

Finally, before making a choice, remember that training and re-training programmers is costly and time-consuming. Also, if your programmers are good at programming one micro, guess which device they'll recommend for their next project? The danger is that software can end up dictating hardware choices, which may no longer be made on sound engineering judgement (component availability, functional suitability, cost, etc). All this lowers profitability, particularly on high-volume products.

Although we'll probably never see a single micro that's "ideal" for all applications, apply the guidelines we've layed down in this two-part series and you will select a micro family that will remain well-supported in the future.

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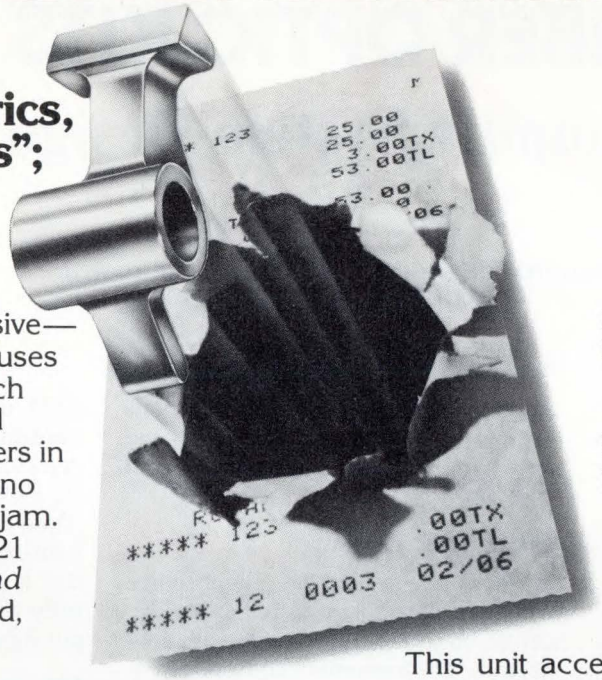

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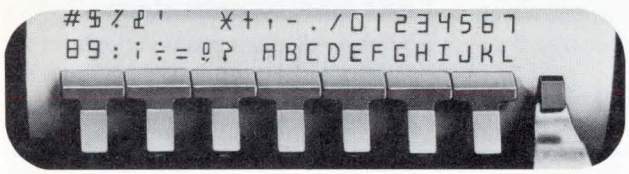

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FIBER OPTIC KITS
Simplify System Design

Leonard F. Bendiksen and Charles Intrieri, Jr.,
AMP, Inc., Harrisburg, PA

Systems designers are now using readily available, low-cost semiconductors to construct low-frequency, short-length dc control and digital communications systems for a spectrum of fiber optic applications, such as medical electronics, POS terminals, petrochemical systems, industrial control, MPU interconnection, security systems, SSR circuits, and dc control and digital communications systems. To show how to assemble a number of fiber optic transmitters and receivers, let's look at several typical examples.

To help simplify experimentation and assembly, a number of manufacturers offer fiber optic kits. For example, our Amp Optimate Fiber Optic Experimental Kit goes beyond traditional capabilities of fiber optic instructional materials and provides semiconductor devices for transmitter and receiver circuits, circuit boards, wave guides, connectors, tools and instructions to build several different fiber optic systems. System designers can construct systems which are both TTL- and CMOS-compatible — which are operational for most low-frequency data links and short-length experiments — and create links up to 20m (for 1 Mbit systems) and as long as 45 m (1 Kbit systems). Other kits are available, and each offers differences, so you should shop around to see what suits your needs. Of course, remember you're not evaluating kits, but are evaluating the product itself for your intended application and possibly also using it for familiarization-education purposes. Generally, if a fiber optic manufacturer has a good product line and support, it should back this up with quality kits.

One word of caution: don't expect a kit to produce "saleable" systems. But it can bring an experimental fiber optic link to about 85% of the way toward a final commercial design. Still needed are environmental protection details such as temperature compensation and the obvious repackaging for production economy.

Fiber optic review

A fiber optic system has a light source and light detector, transmitter and receiver, and fiber optic cable with connectors. The transmitter converts an encoded input signal to dc current, which is then converted to light energy by a LED.

Light energy is coupled from the LED into the fiber optic cable, then transmitted through the cable to a light detector. Low-cost light detectors used as PIN diodes, photo transistors or photo darlington transistors detect the light energy and convert it into a current that is amplified and decoded to faithfully reproduce the original digital input signal.

Fiber optic considerations

The basic design considerations for an operational fiber optic system must include: transmitter optical power, sys-

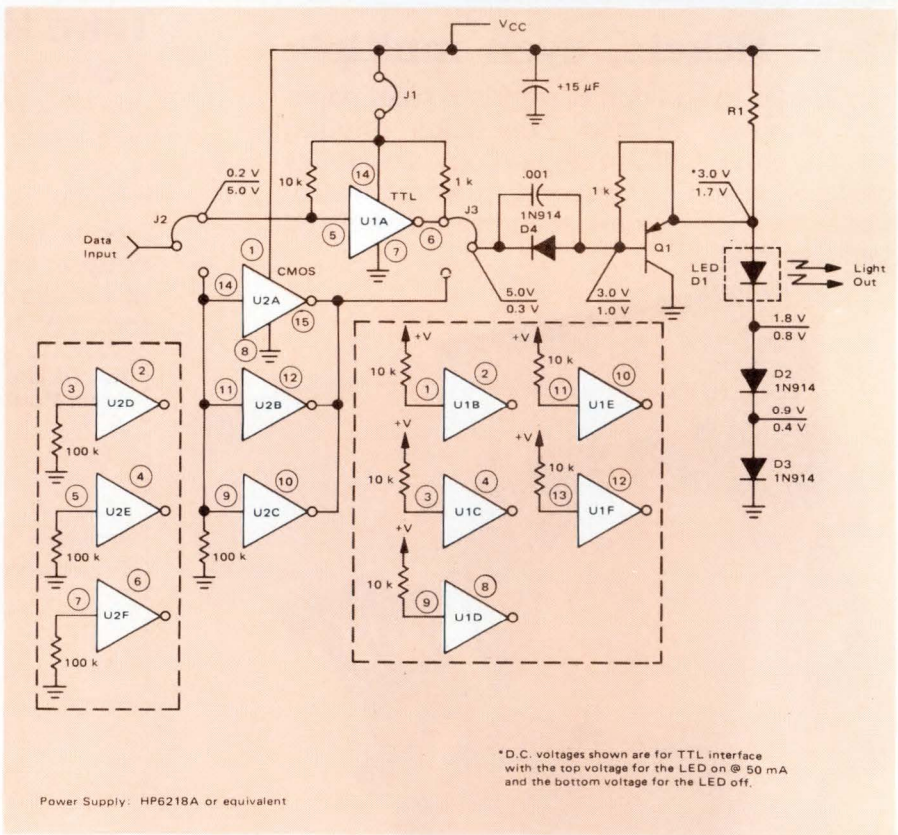

Fig. 1 PC board layout for fiber optic transmitter is designed for TTL or CMOS compatibility. Circuit can be assembled from the following parts list: U1 — SN74LS04; U2 — MC14049B; Q1 — MPS3638A; D1 — MFOE100 or MFOE200; AMP connector — #530564-1, #53028-1.

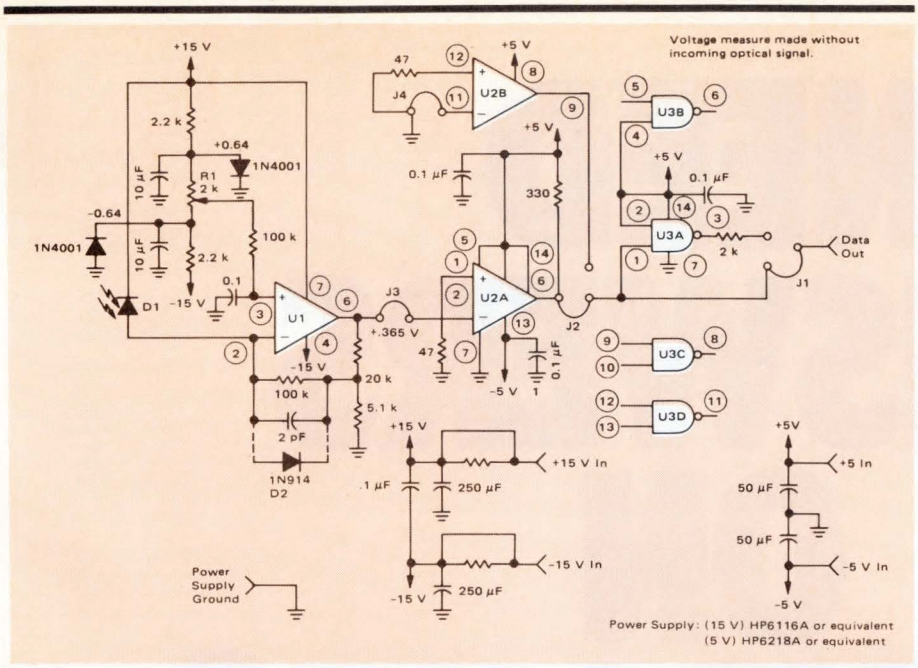

Fig. 2 Megabit receiver schematic and PC board layout. Parts required for the circuit include: U1 – LF357; U2 – MC75107 or MC75108; U3 – SN74LS26; AMP Connector – #530528-1, #530528.

tem losses and receiver sensitivity. Transmitter optical power output (P_T) is usually expressed in microwatt of radiated light energy. The system losses include: LED-to-fiber interface loss, fiber-to-detector interface loss, and fiber and connector losses.

LED-to-fiber interface losses are dependent upon internal LED efficiencies, lens loss, air gap loss, LED spatial radiation pattern, fiber interface surface and their losses. For example, a typical MOFE100 LED-to-0.045″ fiber bundle (with 0.3μ polished surface) interface loss was experimentally determined to be 17 dB.

Fiber-to-detector interface loss is less than the loss at the LED-to-fiber interface. These losses are included in the receiver sensitivity.

Fiber plus connector losses are usually expressed as L_P. Fiber parameters of interest include optical power attenuation and pulse broading. However, for short system lengths and low data rates, the most important factor is optical power attenuation. These losses are expressed in dB and used to determine maximum operational system length. The 0.045″ fiber considered in our examples has an attenuation of 0.63 dB/m.

System length may be determined by subtracting receiver sensitivity from the transmitted optical power (P_T) expressed in dBm. This difference in dB is the allowable fiber and connector path loss (L_P). For a short fiber optic system, with no connector splices, system length may be calculated: X (meters) = L_P(dB)/C_L(dB/m), where X is fiber optic cable length in meters; L_P, fiber and connector path loss in dB; and C_L, fiber attenuation loss in dB/m.

Receiver sensitivity

Receiver sensitivity is expressed in microwatts of optical power. The received optical power is approximately the same as that optical power radiating from the end of the optical fiber. Receiver sensitivity may be more conveniently expressed in dBm. S = 10 log (Pi/1000), where S is receiver sensitivity (dBm) and Pi is optical power (μW) at end of fiber (input to detector).

Minimum receiver optical power required to faithfully reproduce the transmitted digital signal was experimentally determined for each of our example circuits. They are: Mbit receiver — 4.55 μW, 100 kbit receiver — 1.0 μW and 1 kbit receiver — 0.22 μW. Basic examples of typical fiber optic maximum system path lengths (meters) are as follows:

	Path Length		
LED × MTR @ I_F=100mA	Mbit receiver	100 kbit receiver	1 kbit receiver
MFOE 100	6.7	17.1	27.6
MFOE 200	20.0	30.5	41.0

These systems are the experimental fiber optic digital data links that also will be discussed in the following examples.

Building transmitters

The experimental fiber optic transmit-

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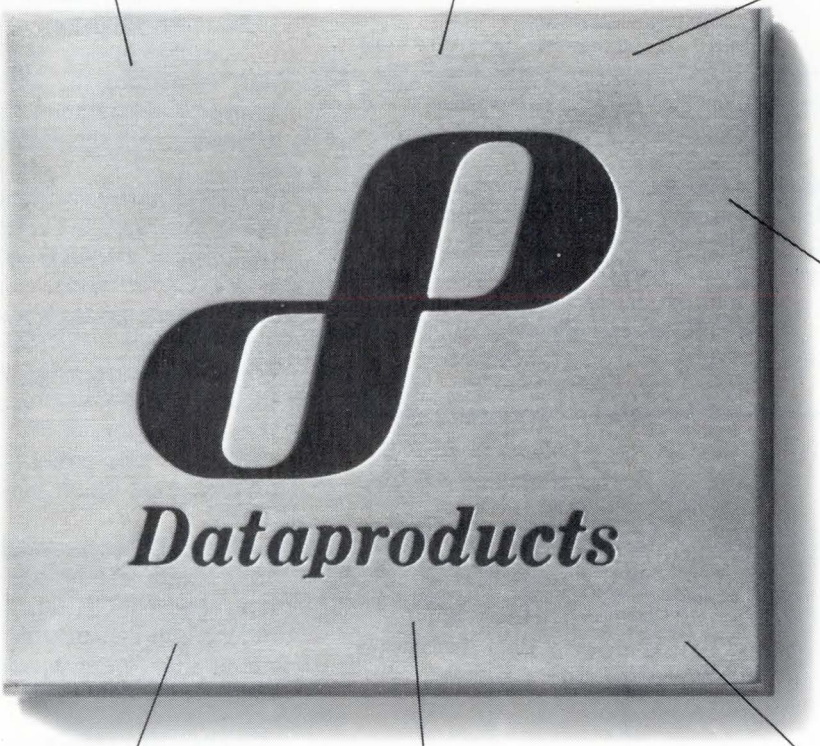

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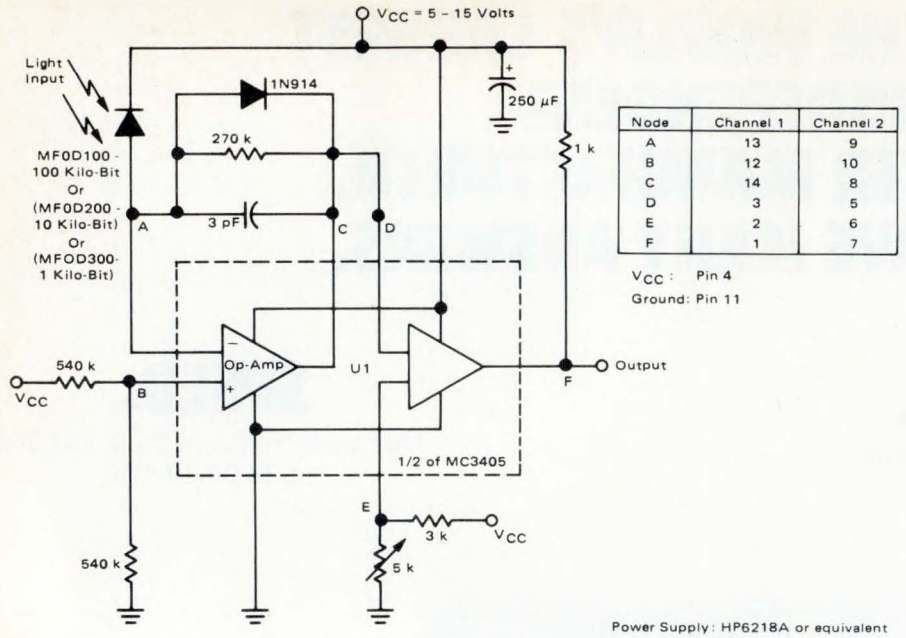

Fig. 3 PC board layout and schematic for 100 kilobit receiver (1 IC/2 channels). Parts required: U1 — MC3405; AMP Connector — #530564-1, #530528-1.

ter (Fig 1) is TTL- or CMOS-compatible depending on the circuit selected (the PC board layout accepts either). The transmitter handles NRZ data rates to 10 Mbits or square wave frequencies to 5 MHz.

The transmitter, which requires only 150 mA, may be powered from a +5V supply for TTL operation. The LED drive current is adjusted to the proper power output level needed for the system by resistor R1. The value of resistor R1 is calculated as follows: $R1 = (V_{CC} - 3.0V)/I_F\Omega$, where V_{CC} is power supply voltage and I_F is desired LED forward current.

In operation, the LED is turned off when transistor Q1 is driven on. Diodes D2 and D3 assure turn-off of the LED, while diode D4 prevents reverse bias breakdown (base-emitter) of the transistor Q1 if the IC's U1 or U2 outputs are high.

For TTL operation, the transmitter is assembled using IC U1 (U2 is not used as part of the assembly). Jumper wires J1, J2 and J3 are inserted to connect to U1 the remaining components.

This transmitter will operate from standard TTL data levels with a power supply voltage of +5V ± 0.25V. An unused section of U1 may be connected as an inverter for the input logic, or the sections may be additional drive circuits for multi-channel operation.

For CMOS operation, the transmitter is assembled using IC U2 (U1 should not be part of the assembly). Here, jumper wires J2 and J3 are inserted to connect to U2 the remaining components.

U2 has three inverters in parallel to drive transistor Q1. Furthermore, U2 performs as a level translator to accept CMOS input levels as high as +15V while operating from a supply voltage as low as +5V. The unused sections of U2 may be used as invertors for input logic or may be used for a second transmitter drive circuit of a multi-channel operation. The power supply for this CMOS transmitter may be +5V to +15V.

The LEDs required depend upon systems length and desired operating data rate. The MFOE100, MFOE200 and other LEDs may be used with the transmitter after careful consideration of rise time, power output, etc.

Assembling receivers

The following are guidelines for assembling both megabit receivers and 100 kilobit receivers. As with the transmitters, the receivers shown in **Fig 2** are TTL- and CMOS-compatible.

The Mbit receiver **(Fig 2)** uses an MFOD100 pin photodiode as an optical power detector, which responds linearly to the optical input over several decades of dynamic range. The optical power to diode photo current conversion factor is 55 nA/μW (typ). 4.55 μW is the minimum optical power to faithfully reproduce the transmitted digital signal.

Minimum PIN detector output current is converted to voltage by U1 (op amp LF357); the minimum diode current required to drive U1 is 250 nA for a

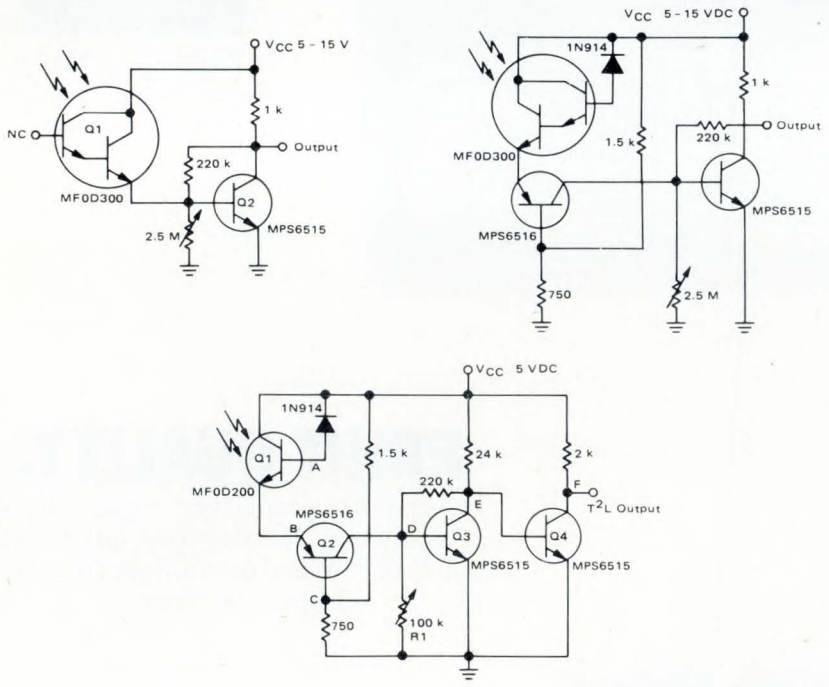

Fig. 4 A simple photo darlington receiver (a) may be used in a dc control or low-frequency system. The output of the MFOD200 drives a single (MPS6515) transistor C-E amplifier. This circuit will operate from a +5 to +15 V supply and its output is TTL/CMOS-compatible. The photo transistor receiver circuit (b) may be used to data rates up to 20 kbit. The receiver sensitivity at 10 kbit is 5.5μw. By adding a second transistor (c), frequency is extended from one to two kbits.

1 Mbit data rate. At lower data rates, U1 will respond to lower diode photo currents. For example, at a 250 kbit data rate, only 100 nA of diode photo current is required. The receiver's dynamic range is extended with diode D2 to prevent U1 from saturating at large optical power inputs.

IC U2 acts as a voltage comparator. Its worst case sensitivity of 50mV determines the size of the pulse required out of U1. U2 detects, inverts and provides standard TTL logic levels to the output. Light at the detector input is converted to a logic high level at the receiver output. C1 and R2 provide a hysteresis loop around U2 and acts as wave shaping to high frequency logic.

CMOS compatible operation is provided when U3 is wired into the PCB. This IC is an open collector TTL quad, two input NAND gate device. Jumper wire J1 must be connected from U3 output to the receiver output terminal.

100 kbit receiver for dc control and low frequency data rates **(Fig 3)** is inexpensive. Although we described only one receiver section here, the unused IC section may be used to generate other circuit functions or may be used for additional receiver circuits.

A single IC two channel receiver (**Fig 3**) uses a single IC (MC3405). which contains two opamps and two comparators. The receiver is TTL- or CMOS-compatible and operates up to a 100 kbit data rate.

Receiver waveforms are similar to those of the two-IC receiver. In both, the single IC diode (D2), in parallel with the feedback resistor (R2), assures that the opamp will not be saturated by larger photo currents.

While these receivers are intended for use with an MFOD100 PIN photo diode, they may also be used with the more light-sensitive, but lower speed, MFOD200 photo transistor or higher gain MFOD300 photo darlington.

For example, a kbit receiver is constructed by replacing the MFOD100 pin diode in either receiver with the MFOD300 photo darlington. Switching speeds of these receivers, using the MFOD200 photo transistor and MFOD300 photo darlington, may be increased by connecting a diode across the collector base junction. If this diode is not used, the base leads should be cut off flush with the transistor header to eliminate possible external noise pickup. DD

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SETTING UP A MICROPROCESSOR DEVELOPMENT LAB

Bill Schweber
Instron Corp.

After you have selected the microprocessor development system (MDS0 for your next design, you may think that the only thing to work on full time is the software and hardware of the new design. This is only partially true. A great deal of effort and forethought is needed to set up an effective development lab. You have to decide on all sorts of miscellaneous support items and anticipate problems to keep the lab and project functioning smoothly and efficiently. Without this, work will proceed slowly or come to sudden halts as you frantically rush around trying to get the missing parts and supplies. Some technical choices must be made early in the project design so that the appropriate follow through is started early.

The goal is to establish a reasonably efficient development lab that will promote getting the job done while minimizing daily frustrations. If the set up in the lab has a lot of kluges and patches, at some point they will start falling apart, just by probabilities alone. Main areas of concern are: 1) MDS supplies, support and debug hardware and tools, 2) PROMs and PROM burners and 3) documentation in the lab environment.

SUPPLIES FOR THE MDS

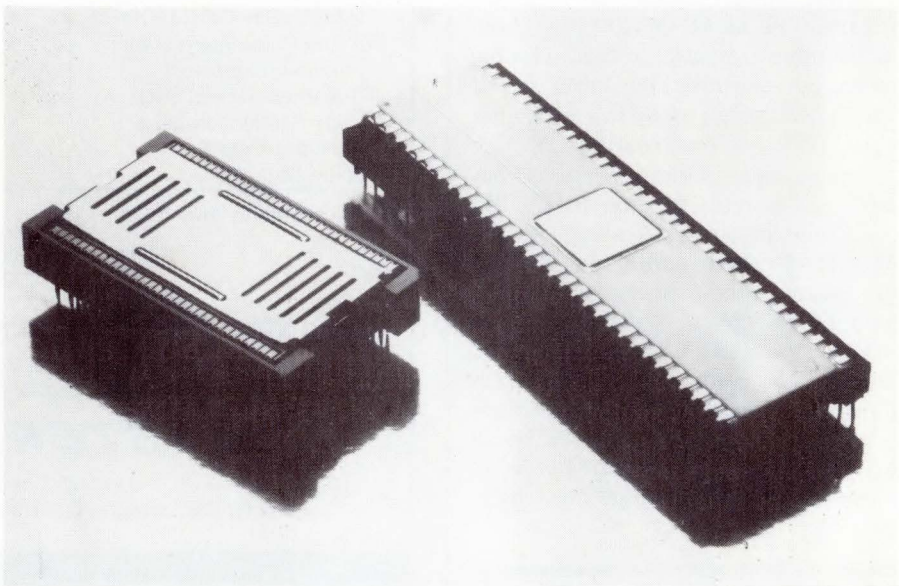
Most development systems use floppy diskettes as the storage medium for software (some use cassettes). The MDS usually has a hard-copy printer or printing terminal in addition to the CRT used for editing, assembling, and debugging.

You can buy the diskettes, cassettes, and paper for these peripherals through computer supply specialty houses and some larger commercial stationary stores. Since diskettes and cassettes are about $5 each — and you will use lots of them for various types of programs (test, operating system, sysem operational, and archival backup) — be sure to order enough, especially if you have more than one person programming on your system. Make sure that you buy diskettes compatible with your drives — hard sectored, soft sectored, etc, and with or without a write-protect hole. The latter is a pre-punched hole that inhibits the disc controller from writing on the diskette, and it can be covered with a tab to allow writing. Get some kind of file or storage box to hold all the diskettes in an organized manner.

Printer paper should also be stocked because it is a good idea to make a fresh listing every few days or once a week, and file away older listings. If your printer is an impact model capable of multiple copies, you will sometimes want to use this feature. Keep a smaller supply of 2- or 3-part paper available so you can make several copies at once. (Most of the time, single-part paper is all you'll want.) You should check your supplies on a regular basis and re-order when you run low, relative to expected delivery time.

Power supplies

The power supply for your μP-based PC boards is an important link in your overall system; if its capacity is inadequate for the load of your cards, the supply could go out of regulation and delivery less than the treated voltage. This is frustrating and causes phantom problems in the circuitry when the lower supply level causes some components to work marginally or erratically (4.75 V for some 5 V nominal ICs).



The new 64 Quad In-Line Package (QUIP) by 3M uses approximately 40% less space on a PCB than an equivalent DIP. No insertion force is required to connect the chip carrier and socket.

Measure voltage at the chips themselves with the system under full load to ensure that supply lead and track IR drops aren't too high; a few amps flowing through supply wires and connectors easily loses 50-200 mV.

The particular power supply voltage and amporage capacity you need depends on the system's type of μP and cards. As a rought guideline, add 1.5-2A of 5V supply for every medium density card of about 7" by 10" (the size of a Multibus card) in the system. (For a system using CMOS components, it is less.) Also check if your system needs any other voltages, such as ± 15, +12 or 24 volts ac. You can make or purchase separate supplies for each voltage, or use a single supply with mutiple outputs of the more common voltages.

Many power supplies are available with overvoltage protection and automatically short the supply output if the level rises by some amount (typically 20% above nominal) which occurs if critical supply components fail — a failure that can easily destroy your whole set of circuit boards.

When setting up the lab bench, in addition to the switch for the power to the MDS and other test equipment, have a separate ON/OFF switch for the supply to your PC cards. When plugging cards or chips in and out of your system, this makes it easier to shut power off.

Extenders and other special cards

Most multiple card μP-based systems use a card cage and backplane to interconnect various system cards (see "special Design Guide: New μP Packaging Options" by Carol Anne Ogdin and Robert Cobaugh in the October and November issues of Digital Design.) Extender cards are essential so that you can run your system with a card physically pulled out of the cage and put various probes on key points. You may also need extender cards to provide clearance to get the emulator cable for your μP into the IC socket. Extender cards are commercially available for some of "standard" backplanes (S-100, Intel Multibus and TI 990, among others). If they are not yet available for your backplane, or you are using a non-standard backplane, get extender cards laid out and fabricated promptly. You'll need quite a few of them.

Extender cards are useful in other ways. If you leave the connector off the extender card, you can solder 0.025 in^2 Wire Wrap pins into the holes where the connector would go. You or your tech can easily connect oscilloscope and logic analyzer probes to any bus signal (instead of awkwardly clipped onto IC pins) saving time when connecting numerous logic analyzer leads to monitor bus acitivity. To aid this, some Hewlett-Packard probes use little grabber clips that can be disconnected from their wires and the wire itself fits directly over the Wire Wrap post.

The test probe pods on logic ana-

lyzers from Tektronix, H-P and some other manufacturers have a built-in connector which mates to the PC card's edge fingers. Do you have this kind of instruments? Then consider laying out a special extender card which picks up selected bus signals and brings them to a card edge physically compatible with the pod connect (Fig 2b).

Connectors and sockets

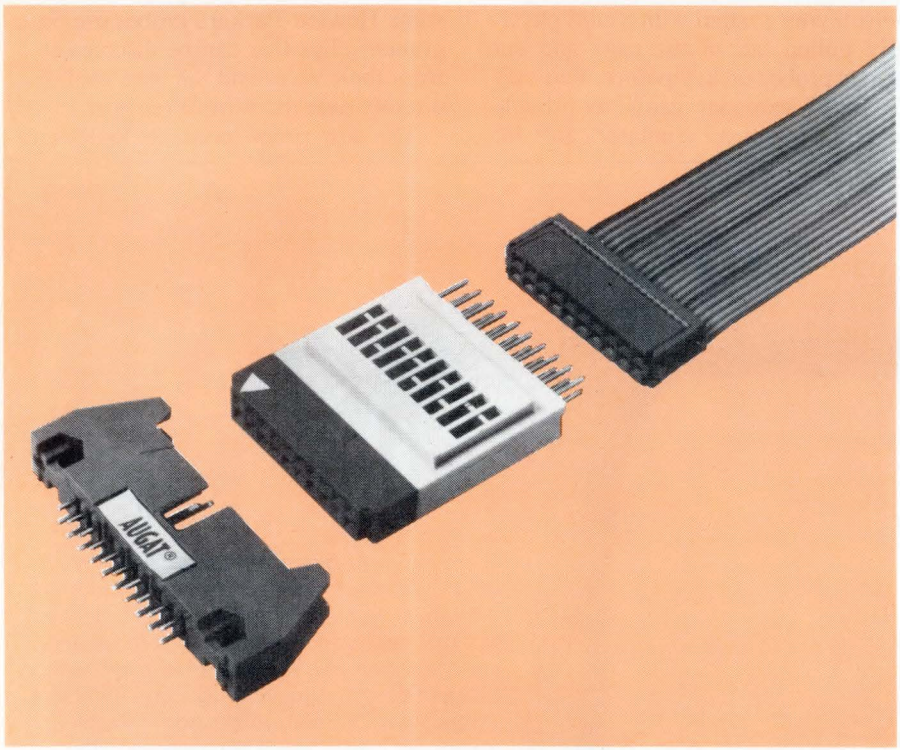
Most edge connectors and IC sockets are rated for reliable contact only within a number of insertion/withdrawal cycles of whatever plugs into them, and a typical 16-pin IC socket could have intermittent contact after only 20-30 such cycles. In the lab environment, it's common to remove and insert certain ICs over a hundred times within several months. These intermittents cause frustration, aggravation and wasted time.

Both zero insertion force (ZIP) and low insertion force (LIF) IC sockets are available, in various sizes from 14 to 64 pins, for most IC DIPs. The LIF has specially formed contacts in which required insertion/removal force is low but sufficient for good electrical contact. ZIP sockets use a mechanical lever scheme to open and close the contacts. Identify PC card chips pulled frequently and replace their sockets with LIF or ZIP types. Unfortunately, these sockets are larger than regular socket, and there may not be room for clearance on a moderate-density circuit card. In some cases, you can manage by soldering the special socket to "stilts" made of Wire Wrap pins themselves soldered into the board.

Similarly, ZIP connectors for the backplane are available, which substitute for the regular edge connectos. (See "Special Design Guide" Part 2, Digital Design, Nov. 1978.

You should also get a supply of heads (carriers) and elevator sockets. These plug into an IC socket and bring the socket pins up into the open. They enable you to deactivate some pins of the IC, and cut the signal to some subfunction, (for example, to disable a feedback loop in the hardware for checkout or to hang a probe on some lines).

Also be concerned with removing ICs from sockets — use a proper IC puller to preserve the component pins. If you use your fingers, X-acto blade or screwdriver, sooner or later you'll bend pins (which sometimes break when bent back).



The Intra-Switch provides for line-by-line diagnostic testing or quality assurance for flat ribbon cables. Positioned between the female plug on the end of a flat ribbon cable and a male plug on a header assembly or an Intra-Connector, the device has individual sliding switches that open and close each connection between its male and female sides.

Cables

It's been said that a cable is a source of trouble connecting two other sources of trouble. Both the MDS and the system you are developing use cables.

Most peripherals to the MDS are interconnected by a cable with a 25 pin D-shaped connector at either end, commonly called an RS-232C cable after the Electronic Industry Association (EIA) standard it is supposed to meet. Sometimes a few wires must be interchanged within the cable so that the MDS and peripheral can communicate properly. (If you make up any specials like this, be sure to mark the needs with a tag so you don't use the cable in place of a standard one later and then wonder why the equipment doesn't work.) Usually the interconnection cables will have pin connectors (male) on both ends. You should also have cables with pins on one end and sockets (female) on the other, to use as "extension cords" to the original cable, as well as in those cases where the socket is required.

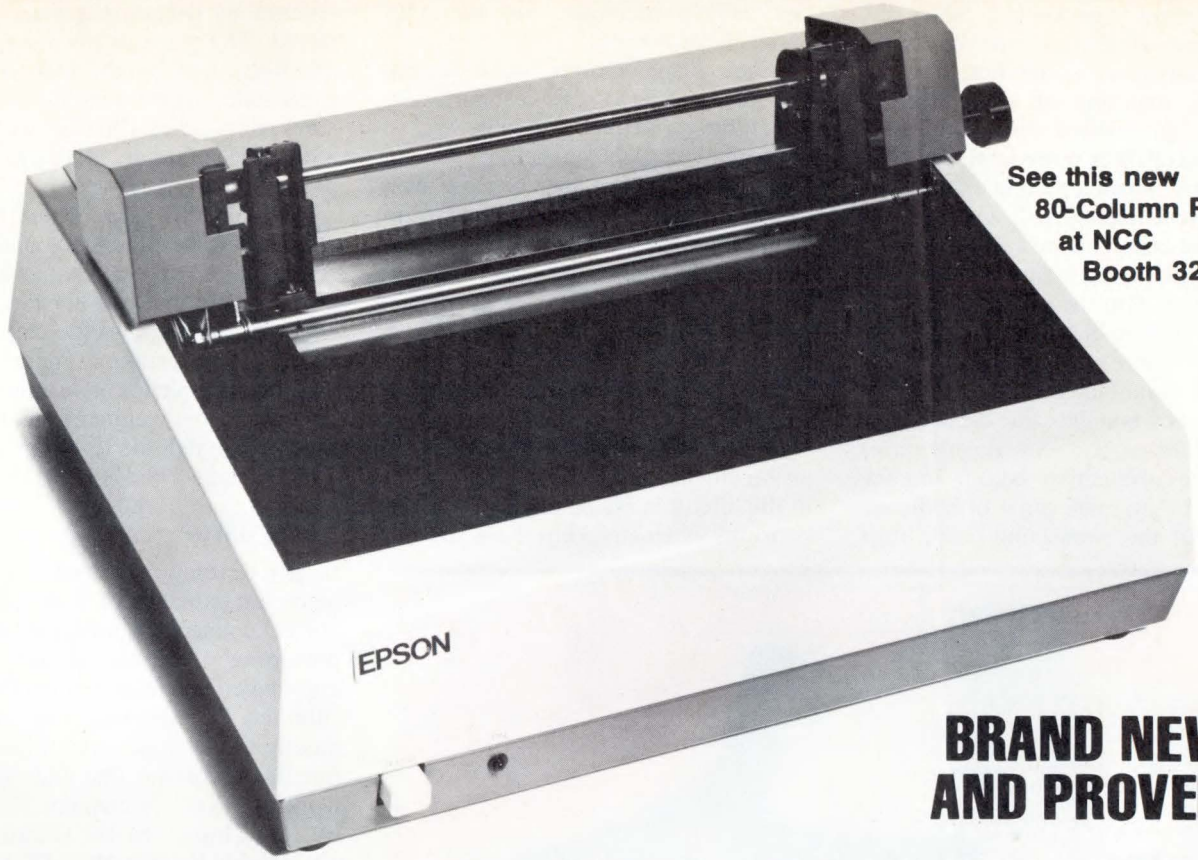
If a single peripheral is shared by two or more systems (as in the case of a fast line printer serving multiple MDSs), get a switchbox control that allows switching the peripheral between systems without connecting and disconnecting the cable constantly, which could produce intermittents. Such boxes are available for switching between two, three or four sources and are useful in the reverse case: when the MDS has several printers available — one of which provides single copies, and the other multiple copies.

The D-style connector also includes provision for locking screws. Use these to screw the cable and hardware connector together; otherwise, the weight of the 25-wire bundle can pull the connectors apart.

Mass-terminated flat cable, used in many μP systems to handle most non-bus connections (sometimes also used for the bus), is popular because of the high connection density and ease of making up cables without wiring mistakes.

Three flat cable termination types exist: (1) The **edge connector** mates with the fingers on the PC board edge and is often used because it saves space and the cost of a mating connector (2) The **socket connector** mates with square pins or a matching header (used where locking against pull is needed or edges are unavailable (3) The **solder connector** solders directly into the circuit board.

In the lab it's a good idea to stock all three types in the widths you will be using on any of your circuit boards or system. You will often have to make up



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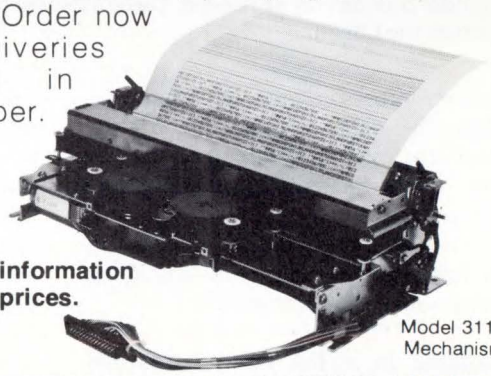

Model 3110 Mechanism

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longer cables, special test cables and transitional cables from one type of flat cable temination to another. The flat cable terminations are available with strain relief, which you should use (even though it is more work to make) so that the constant pulling on the cable when disconnecting will not cause the connector crimp on the cable to break.

Physical keying to prevent connector installation with the wrong orientation is a nice feature but may be impractical in the lab where many different connector/cable combinations are needed (and sometimes when the same cable is used in different places). So, double check the cable orientation before installation, and then mark pin 1 of both connectors of the connection (with black marker, press-on dots or whatever). When the cable consists of an edge connector mating to circuit board fingers, mark the connector and board prominently. Get into this habit of marking every non-keyed connector in the lab and you will avoid damaging equipment by misconnection.

The RS-232C D-connector is also available in a flat cable terminated style. If you keep some of these in both pin and socket variety in your lab, you make up, as required, extension cables or short cables to change a socket-type cable end to pin type (or vice versa), or to connect to longer cables with the same sense of end together. However, the flat cable type D is in convenient when some wire assignments must be interchanged within the cable, so that flat cable's automatic accuracy becomes its drawback.

Some manufacturers make special flat cable connectors, for test purposes, which bring out each flat cable lead so you can put a probe on the line, or with switches so you can open or close each individual line — both difficult to do with flat cable. Unfortunately, these special test connectors come only in limited sizes.

Logic Probes and clips

When using a relatively expensive MDS, it's easy to overlook the need for a very basic logic probe ($30-$100). A probe quickly indicates if a logic point in the circuit is HIGH or LOW, which is useful when checking if the μP can control output lines and set certain control lines. Many of the probes can also detect if a single short pulse occurs and provides a visual indication. But be carful; the shortest pulse a given probe can detect may be longer than the pulses for which you are probing, and you may think incorrectly that the pulse isn't there.

A less well known (and more expensive) complement to the logic probe is the logic pulser. Instead of sensing and indicating the state of a line (as does the probe) the pulser forces the logic line to go to the opposite state of its present state. It overrides the existing state but does not damage the circuitry. A conventional "pulse generator" cannot do this properly and safely. Some of the logic pulsers can select 1, 10, 100 or a continuous stream of pulses to be injected. The pulser is invaluable for stimulating stuck circuit nodes to the desired state, clearing circuit latches and gates, or toggling flip flops, all without requiring action by the software and possibly faulty hardware.

Also, get IC clips which resemble oversize clothespins and grab onto each side of an IC, making contact with each pin, thus letting you hook scope and analyzer probes onto the chip without shorting adjacent pins. These 14-, 16-, 24- and 40-pin clips have a small disadvantage — the weight of the probes on the clip can pull the IC out of its socket a bit, causing a bad connection.

Spare parts

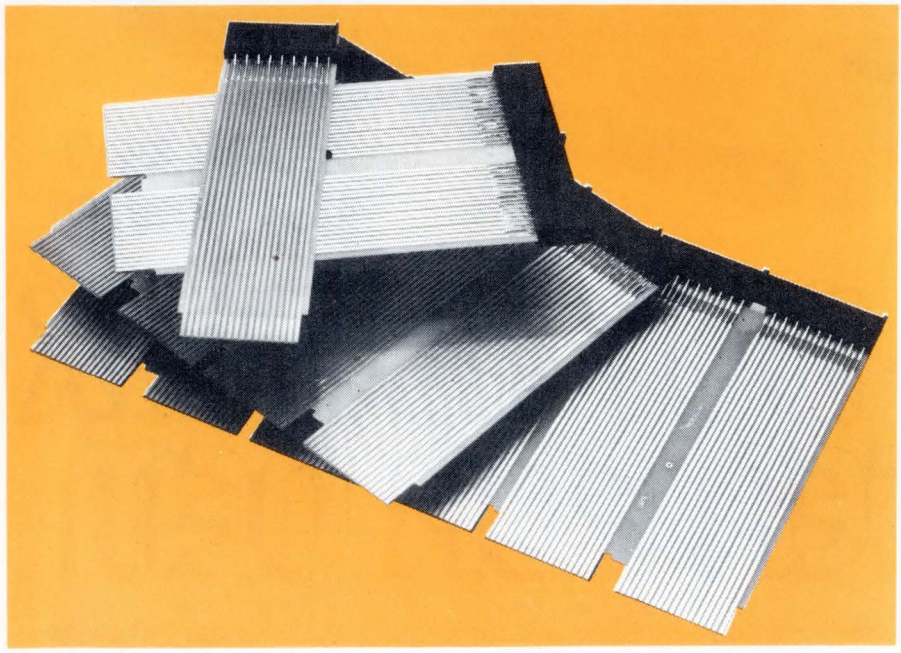
In any developmental activity components are damaged or destroyed by incorrect connection, mistakes or "probe poisoning", and not all parts will be good when you receive them from your supplier. Be especially wary of multifunction LSI chips, which have some functions working fine and others not working. (See "Viewpoint: Beware of Buffalo Chips," by Dr. George Atkinson, Digital Design, Nov. 1978, p. 96).

Keep spare supplies. The power supplies for you system are always vulnerable since voltages they supply are physically present in many areas of the circuit cards. Supplies are usually repairable, but it takes time to get components needed or send the unit back to the factory.

Spare circuit boards for each board in the system are also a good idea. They allow you to replace or substitute when you believe a board has failed peculiar to one set of components of the board. Once you know which board is bad, you can spare time to repair that board with spare chips.

The chips most likely to fail or be damaged in a system, because of the role they play, are the I/O chips, buffers to other boards, and optocouplers. R/W memory chips may also fail internally, either in a few locations or blocks of locations. Basically, you should have spares on hand for, or quick access to, nearly every type of component on your boards, with a greater proportion on the most electrically exposed components.

In theory, with spare boards you really don't need spare components, and vice versa; in practice, you need a lot spare boards to support your maintenance if done at the board level only (and tossing a lot of almost good ones on the scrap heap): On the other hand, repairing at the component level can be



Extender boards may be needed. These extender boards are used in DEC-type backplanes (such as the LSI-III).

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very time consuming, especially in the midst of system and software debugging. So, stock both for efficient operation.

Before replacing any circuit board or component, perform obvious checks on the supplies feeding that board or component. If the 5 V supply has gone up to 6 v, it will ruin the replacement too.

If your PROM is of the fusible link type, you will need lots of extras since once burned they cannot be changed. You will probably be burning several preliminary PROM sets before the final one, as well as making sone mistakes while learning to use the MDS and PROM burner combination. If the PROMs are erasable (EPROMs), you won't need as many extras. But you would still be prepared with some since the erase time under the UV lamp is about 1 hr. Be sure you have the proper type of UV lamp for your EPROMs (typically, output is in the 2537A region) and know your lamps' strength (from the lamp sped) so you know the required erase time and distance. Understand the safety rules for these lamps; safety goggles are a good idea.

Burning the PROMs

The main objective in burning PROMs in the lab is to get the first set done; Duplicates are easier to make on any PROM burner (or outside vendors can do it).

If your final program is relatively short (under about 256 bytes), you can enter data into the PROM via the PROM burner keyboard. But beyond 256 bytes, it's impractical. The MDS should be capable of communicating with the PROM burner and loading the desired object code into the burner. This is no problem if the burner is an integral part of the MDS: if not, the linking may not be so simple. Even if both the MDS and PROM burner use the same interface, such as RS-232C, this only defines the hardware aspect of the interface, but not the format and protocol used for transmitting the data. Different protocols are in use today, including Fairchild Formulator, MOS Technology, Motorola Exorcisor, Intel MOS, Signetics absolute object, ASCII-BNPF, and others. If not the same, you may have to write some software which reformats the data being transmitted (assuming the hardware interface is free).

Labeling PROMs

Don't remove a PROM from the PROM burner until you stick a self--sticking label on it. This sounds simple and obvious, but it happens all too often, with burned and unburned PROMs completely mixed. Self-stick paper labels used for manila folders and envelopes are easy to get, inexpensive, stick well to the chip and don't fall off when the PROM gets hot. Since labels often cover the IC pin identifier, mark pin 1 on the label so the PROM won't be plugged backwards into the socket.

Hardware simulators

Many μP-based systems will be connected to some external circuitry as part of the overall configuration of the final system. This circuitry may have switches, lamps, analog voltage signals which may be digitized and perhaps mechanical devices (motors). A simulator is a simple piece of hardware which tries to look to your system and software like the final external circuitry, but is easier to build and control.

For example, your system may, as part of its data acquisition, digitize the analog voltage from an external transducer, and also output a logic level to an indicator if the voltage passes a certain point. Rather than connecting the actual external hardware (which may be large and awkward), you could use a voltage source (battery or ac supply) and a multiturn potentiometer to simulate the incoming level, and an LED indicator to monitor the output logic level. The pot lets you vary the input voltage slowly and in different patterns and check, at a first level, if your software algorithms can handle the different input characteristics.

As another example, if your system is to receive and transmit parallel data, with control of a few handshake lines, you might construct a simulator with switches to set in the data to be presented to the input port and LEDs to indicate the logic levels of the lines of the output port. Some simple circuitry would take into account the status of the control lines and integrate that with the switches and LEDs.

Remember that a simulator is only a coarse approximation of the real system. As you try to make the simulator more realistic and valid, it will take additional design effort and soon reach the point of diminishing returns. Also, the simulator is just a physical realization of what you think the real hardware will do, and you may be unknowingly making incorrect assumptions. However, the simulator can be very useful for checking out the μP system interfaces and basic software routines for handling I/O and data, especially if building the simulator involves only some switches, indicators, logic gates and voltage sources.

Maintenance

MDS equipment should be on a planned maintenance schedule to decrease unexpected breakdowns, which usually occur when everythng else goes wrong.

All lab maintenance involves units with motors and other moving parts. Check the disc drive or tape transport manufacturer's specs for the recommended frequency of cleaning heads (for tapes) and checking bearings and aligning them if needed. Printers and printheads should also be checked and cleaned in accordance with the spec. The air filters over cooling fans in the various pieces of equipment should be cleaned on a regular basis, since a decrease in airflow (as a result of dirt) increases the failure rate of equipment components.

Time required for regular maintenance is small, typically a few hours/month, so the time spent will be worthwhile.

II PROMs and PROM burners

Marketing and design requirements for many μP-based systems include PROMs used to hold the program that the customer will receive, rather than tape or disc. Once the engineering group picks the particular PROM to be used, on the customary tradeoff involving cost-speed-power-density, it is essential to be prepared to actually burn some of these units.

The PROMs themselves should be ordered well in advance of the date they will be needed in the lab. There are literally hundreds of different PROMs on the market, and due to large demand or low supply, it may take longer than you would normally expect to get the ones you select.

Some designers and techs place names on these labels, but this clutters the label. Instead, use sequential numbers corresponding to a PROM description and comments (e.g., is it an update of a a previous PROM?) If the PROM is small or a decoder for addresses, include a printed listing of what's in it. There's a final advantage to using numbers for PROMs; these first PROMs (which often form a a master set for future copies) won't accidentally get put in a unit that's shipped to a customer. (Those PROMs will have a production number, instead.)

DOCUMENTATION

μP development lab documentation is different than the formal documen-

tation that engineering provides to the manufacturing organization when a product design is complete. In the lab, there's a large number of special cables, boards, adapters, temporary jumpers and modifications. Some are used only in the development lab; others will accommodate temporary design errors or unavailable components.

Some designers keep track of all these specials by memory (or word of mouth). Don't! Mark each cable, circuit board or adapter with a number and keep a logbook. Note the items' date, nature of the special or modification (track cut, output leads swapped, cable wire left open) and the reason. If space permits, put a detailed tag on the item. Don't rely on them as they can't tell the full story and may be a nuisance.

Software Documentation

The software documentation problem is usually discussed from one perspective: how to document the final software so it can be expanded of debugged when field reports come in.

In the development lab, your people must document all intermediate software prior to completion. Get careless and a lot of old, not-quite-accurate files and listings will accumulate. To prevent this, periodiallly generate a new, complete listing of all code — every few days if you generate a lot of new code; once a week if slower. Mark the date prominently on each listing and keep theolder listing in a central location. Work only from the latest listings and use older ones only for reference or comparison. Of course, some programs which are modified less frequently (such as those used for test purposes or hardware exercisers) should be kept in the central file, with new listings generated when changing programs. Keep previous listings for comparison.

Does setting up an effective μP development lab take constant work and effort? Yes, it's inevitable, but you can minimize frustration and aggravation by following the common-sense rules we've presented. DD

ABOUT THE AUTHOR

William Schweber, a senior electronic engineer at Instron Corp., designs μP-based controls for materials testing equipment. Bill obtained his BSEE from Columbia Univ. and his MSEE from the Univ. of Mass.

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COVER FEATURE

TERMINAL OPERATING SYSTEM Offers Unique, Functional Hooks and Handles for the OEM

Mark Crowley
Perkin-Elmer Corp., Terminal Div.

An Overview of Petos Basic

PETOS Basic is a full-feature Basic interpreter for the M6800 family, running under the PETOS Operating System. Its features include the following.

1. Runs under the PETOS OPERATING SYSTEM.
2. Divide by zero produces HALT with error.
3. Matrices with up to 255 dimensions.
4. IF...THEN...ELSE and nested IF... THEN...ELSE.
5. Direct (immediate) execution of statements.
6. Error trapping.
7. Four variable types: Integer, String, Single Precision Floating Point (7 digits) and Double Precision Floating Point (16 digits).
8. Full PRINT USING for formatted output (includes asterisk fill, floating $ sign, scientific notation, trailing sign, comma insertion.
9. Extensive program editing facilities via EDIT line command, RENUM, AUTO, etc.
10. Trace facilities (TRON, TROFF).
11. Ability to call assembly language sub-routines.
12. Boolean operators OR, AND, NOT, XOR, EQV, IMP.
13. Full support of PETOS Device Independent I/O and File System, including both Random and Sequential I/O to either disc.
14. No variable name length restrictions.

Today we see an exploding market for very specific, application-oriented work stations. This new generation of micro and mini-based work stations for lab instrument, POS, transaction processing, or other applications do not need all the end-user bells and whistles found in so many of today's intelligent terminals. What is needed are more functional features useful for the custom integrator.

For intelligent terminals, if there's an agreed upon definition of functionality in the market place, it's one which implies "end user and data entry." But there is a large, emerging OEM market for application-specific work stations for which the typical intelligent terminal is too inflexible and over-priced. This market cannot realize its true potential until there are more devices available which are designed to be effectively tailored by the OEM to the requirements of specific types of workstations.

These OEM-oriented intelligent terminals, or data stations as some manufacters are beginning to call them, are specifically designed to meet the needs of the OEM workstation builder. Among these needs are: (1) Price-performance features that are relevant in a work station environment, (2) Hardware and Software provision for OEM added workstation devices like bar code readers or OCR wands, (3) A human engineered package design that permits the OEM to optimize the work station layout for the application, (4) Software that provides for ease and speed of implementation of application programs and (5) Software that provides a very "friendly" environment to the workstation user.

A data station adds compute power to the modern CRT's human engineering and fine display qualities; provides on-line, fast-access mass storage capabilities; is equipped for the OEM's wide ranging communication requirements; recognizes the necessity for additional hardware devices in a functional hardware/software package. Using this simple definition, many intelligent terminals on the market fail the functionality test (for OEMs), primarily because they are end-user oriented products.

Beaver OS

To better understand how a data station can impact the OEM's product development, let's begin by examining the fundamental element — the operating system — for Perkin-Elmer's Data Station, the Model 3500, also known as the Beaver.

Inherent in terminal operating system design must be expedient methods for using terminal resources, a simple straight-forward OS/user interface and efficient means of task/IO interface. Optimum design features such as these greatly reduce the time needed to complete an OS service request.

The Perkin-Elmer ROM-based Terminal Operating System (PETOS) is a multitasking disk operating system composed of nine major modules: System Manager, Executive, Device Manager, Device Drivers, Timer, Interrupt Manager, Utilities and Diagnostic Manager.

System Manager

The system manager is the user's path to the executive. Its primary function is to accept and initiate commands to the operating system and to control output to the system console. To remove any possibility for operator confusion, all Beaver commands and system messages appear on the 25th display line — the system console line.

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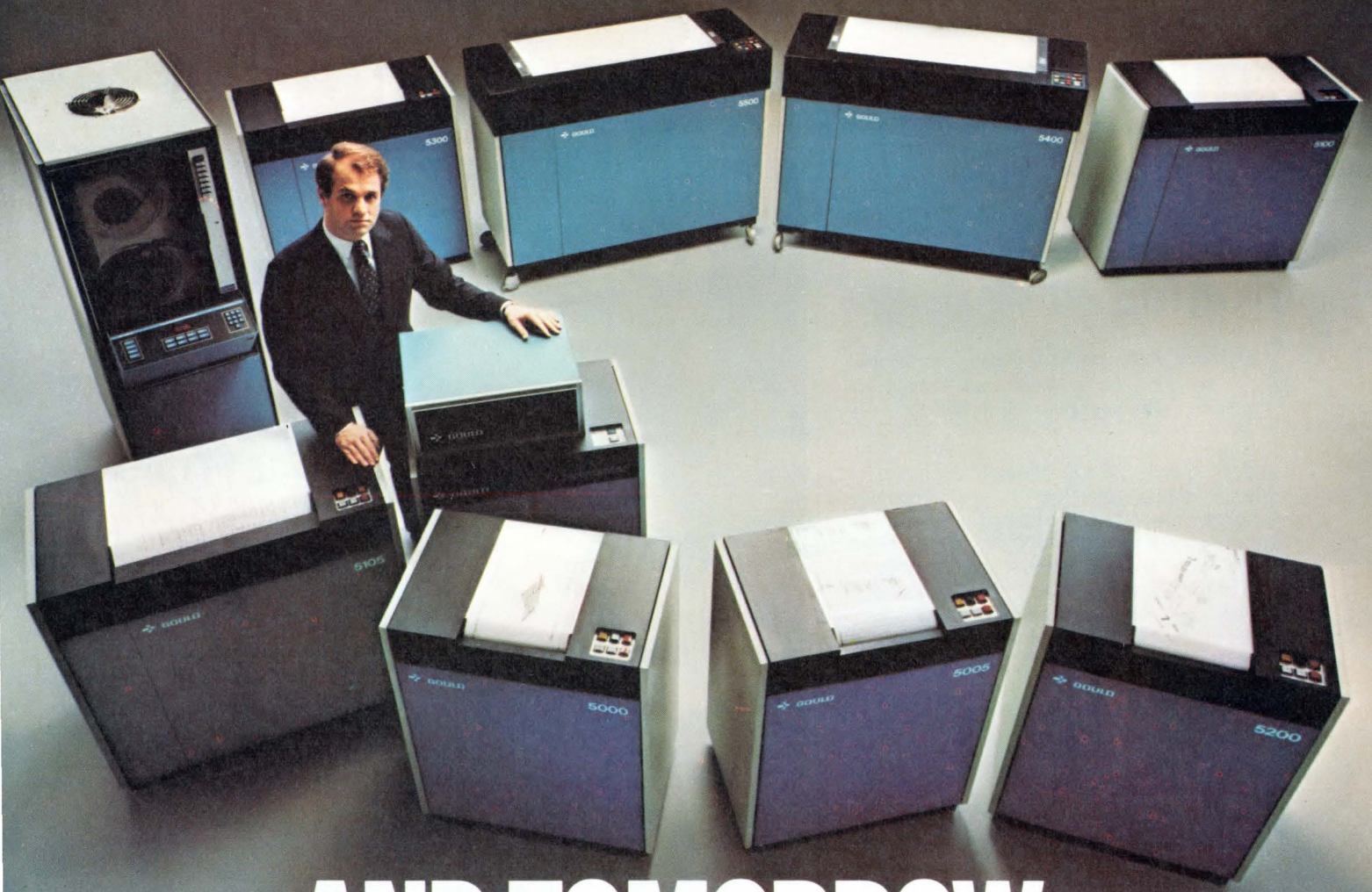

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To perform this mainline function, the system manager controls the sharable keyboard, disconnecting it from tasks to permit new job initiation and permitting round-robin access to active tasks. Keyboard commands or disk files of command sequences using the command substitution system are recognized by the system manager and translated into meaningful system I/O instructions. In addition to dialog between the user and OS, the system manager controls the implementation of the 24 special function keys.

Executive

The executive is the top layer of control for any system resource. When a task requests something, the executive examines the request for obvious errors, omissions or other reasons why the request cannot be honored, but passes the request along to another system module before getting too involved with the specifics of each request. Though the executive does have control over all terminal resources, it gives away some of its power to the device managers.

The executive's primary function is to keep the multi-task environment running smoothly. Every task controlled by the executive is in one of four states: READY, ACTIVE, WAITING, DORMANT. The executive determines when a task must be stopped, whether it is waiting for a resource and when to start another task. At the same time, if another task has completed its I/O, that task becomes ready and control's returned to it.

An active task is executed until cancelled, completed or interrupted. If cancelled or completed the task becomes DORMANT. When no task is ACTIVE, PETOS determines which READY task is to be activated based upon the highest priority. A WAITING task that has been interrupted, will be returned to an ACTIVE state when conditions for continuing execution are met.

I/O Manager

Functioning as a controller of all I/O operations, including screen and keyboard operations, the I/O manager execute I/O request in a prioritized FIFO manner, for each device, providing the different device managers with the information needed to perform their I/O functions.

As the executive passes control to the I/O manager, a task is placed in a wait state, saving the variable and pointers which must be preserved. The I/O manager decides whether the device has already been assigned and whether it can be reassigned. If a problem or previous assignment is encountered, it informs the task through the executive.

The I/O manager also recognizes that a file description has been passed and decides to go to the device manager for the specific disk, or that the call pertains to an actual device such as a printer or communications port.

Through the use of logical unit I/O, the PETOS I/O manager supports both I/O WAIT and I/O PROCEED calls. Since I/O requests are queued, it is possible to set up many reads or writes at one time.

Device Managers

The device manager is simply an interface between the I/O manager and the device driver, though it is here that all the specific, special functions are decoded and where all operations occur.

PETOS provides six device managers, to perform initialization, maintenance and cleanup.

There are managers for the screen, main and auxiliary communication ports, and the disks.

I/O Processor

Because OEM's frequently require application specific hardware, there is one very important, additional manager available. The I/O Processor (I/OP) manager controls a high performance 100KB bandwidth DMA interface to the operating system. This interface board has READ/WRITE protocol and device name. The I/OP greatly simplifies the job of interfacing special peripherals with the operating system and eliminates processor interference because of the M6800 supplies with the interface.

Device Drivers

The BEAVER Data Station differs from previous OEM building-block devices in several significant ways. The microcomputer or minicomputers used in work station design generally are intended to be buried within someone else's product. The BEAVER, while it performs the same functions as the mini or micro, is supplied with ample room into which the OEM can add his application-specific software and hardware.

One way PETOS simplifies hardware changes or the addition of application specific hardware is the provision that the device driver is the only place the system looks at the hardware. This enables the systems designer to add only a device driver when adding hardware.

A device driver contains all device-dependent code and works with one task at a time: a single I/O request, a single I/O control block. Just as there is device independent I/O — I/O can essentially be changed in managers at assign time — so can the user direct output go from a program originally written to work for the screen, to a printer, or another device.

Interrupt Manager

An interrupt causes an ACTIVE task to be suspended and control passed to the interrupt manager. The primary function of the interrupt manager is to determine which device caused an interrupt and pass control to the appropriate device driver.

More manager modules and built-in diagnostics

Other major system modules include the Timer and a diagnostic manager. The Timer permits the request for and cancellation of a timer. Commands are provided which cause an interrupt to be serviced or a timer flag to be set. The timer function also provides a time of day clock, the value of which appears on the display's system console line.

The diagnostic manager contains a self-test feature which exercises all RAM areas. It also allows the setting of breakpoints, single stepping and the examination and modification of memory and processor registers.

Other O/S Software features

The ultimate objective in the design of a data station operating system is to provide efficient, simple and unambiguous use of the terminal as a resource: a building block for the OEM. This implies not only the presence of features which will enable the OEM to make his product as operator-proof as possible, but also product development aids. PETOS does this.

By providing error trapping, the interception of error messages from the system in both BASIC and assembly language application programs, the BEAVER permits the programmer to perform necessary remedial action. A pre-determined error routine can be entered to simplify the operator's job, or simply replace the operating system error message with an application-specific message or instruction. Even without this error interception facility PETOS is geared toward the user: all system error messages and status information are presented in non-numeric, English language phrases. So even messages your programmer cannot control, such as those from utility programs, are designed not to confuse the operator.

Again, both the OEM and end user benefit from the conveniences offered by the command substitution system (CSS). Not only can the OEM provide

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   Wayne Martin
   Methode Development Co.
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2. **"Thick Film Components on a PCB"**
   Dr. Murray Spector
   Alpha Metals
   Newark, NJ 07105
3. **"Miniature PCB's Application in Hybrid Technology by Use of CAM"**
   Larry Fritz
   Microelectronics Technology Corp.
   Palo Alto, CA 94303
4. **"Robots for PC Assembly"**
   Lawrence Kamm
   Modular Machine Co.
   San Diego, CA 92110
5. **"Automotive Applications Using Polymer Thick Film on PCB's"**
   Gerald Keitel
   Methode Development Co.
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DESIGN AUTOMATION —
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Redac Interactive Graphics Inc.
Littleton, MA 01460

1. **"Minimization of Thru-Holes and Circuit Path of a PC Board by Computer-Aided Design"**
   Sam H. Chung
   GE, Aircraft Engine Group
   Cincinnati, OH 45215
2. **"Sprint: A System for Interactive Design of Printed Circuits"**
   Dr. W.M. van Cleemput
   K.R. Stevens
   Stanford Linear Accelerator Center
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3. **"Auto-Interactive PCB Design"**
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4. **"Classification of PCB Types for Cost-Effective Solutions"**
   Jerry T. Harvel
   Markrevel Inc.
   San Diego, CA 92111
5. **"CAD/Artwork Service: Problems and Trends"**
   Dr. M.G. Fassini
   European Institute of Printed Circuits
   Zurich, Switzerland
6. **"A Mature Design Automation System for PC Layout"**
   Henry Bollinger
   Automated Systems Inc.
   El Segundo, Ca 90245
7. **"Interfacing CAD and Manufacturing"**
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   Applicon Inc.
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1. **"PC Laminates: What and Why"**
   Victoria R. Allies
   GE
   Coshocton, OH 43812
2. **"The Effect of Water Incursion on Glass Reinforced PC Laminates"**
   D.J. Vaughan
   Clark-Schwebel Fiber Glass Corp.
   Anderson, SC 29622
3. **"Factors Which Influence Dimensional Stability of Multilayer"**
   Dr. B.Q. Ballert
   GE
   Coshocton, OH 43812
4. **"Effects of Flame Retardant Additives on Thru-Hole Plating of FR-4 Laminates**
   Dr. J.T. Bartholomew
   GE
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5. **"Peel Strength After High Temperature Bake"**
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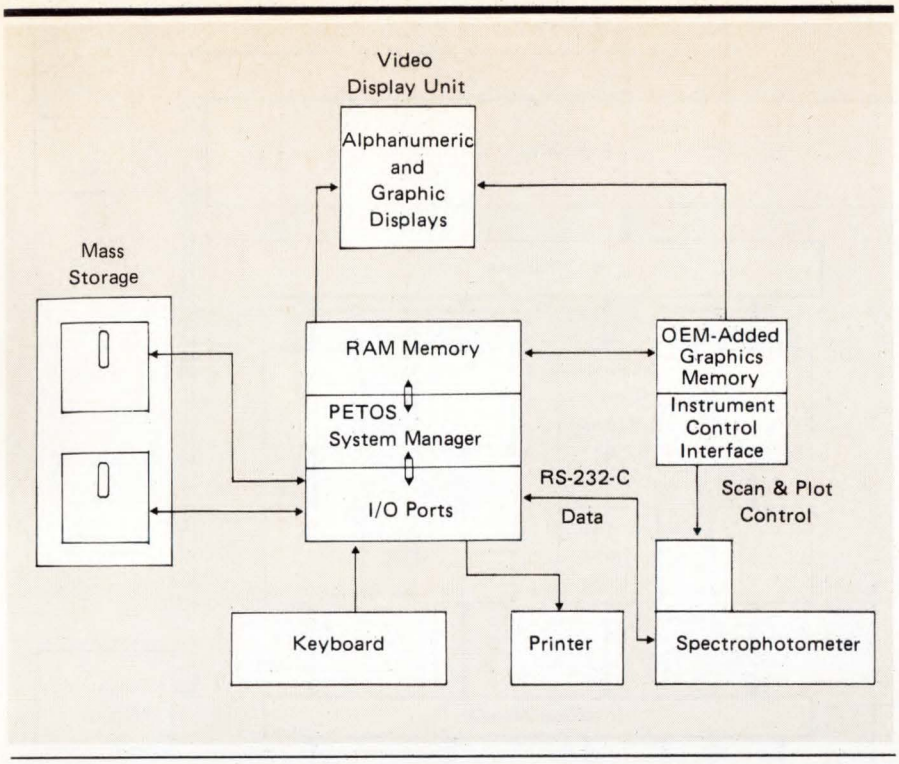


Functional block diagram of the Beaver as used in an Infrared Data Station. The Data Station's functional design permits easy addition of OEM-added hardware and control software.

simple, one-key initiation of complicated procedures for his customer, but the end user can easily tie together frequently run sequences of procedures with CSS. For the OEM, load-and-go procedures can quickly be set up for any new program or system under development.

In any user-oriented end product, the file management and maintenance capabilities are extremely important. The OEM can waste much time perfecting this feature if it is not provided, but PETOS has a field-proven file management system to handle every file allocation, deletion, truncation or update requirement.

Development Features

One of the more powerful development aids provided by PETOS is the DEBUG facility. The programmer is permitted to set multiple breakpoints and can easily produce 'snapshot' dumps. Program memory and register contents can be examined and interactively altered using the PETOS debug routine. A special hardware debug option permits the display of the last 128 valid memory accesses to the processor. Other development aids include a macro assembler which produces BASIC-callable assembler sub-routines, a built-in line editor for programming and file maintenance and a task generator.

User/OS interaction

The data station user interface consists of special keyboard function keys, operator commands and PETOS supplied application utilities. The special function keys include 24 user-definable keys which may be used to start programs and remote devices or to retrieve from disk and execute complex sequences of CSS commands. Other function keys clear the screen, set the tab, reset errors, switch the sharable keyboard to another active application task, or put the keyboard in communication with the system.

In addition the normal operator commands to START, CANCEL, LOAD tasks or ALLOCATE, RENAME, DELETE and DISPLAY files, PETOS provides four functional utility programs, in the easily understood, operator command format: BACKUP, DUMP, COPY, and DIRECTORY. With BACKUP the user generates new disks, provides application or user-specific disk names and has several options to copy and verify the exact image of whole disks and system files a backup file. File reorganization is also a function of the BACKUP utility.

The DUMP utility provides a convenient means of examining or modifying the contents of any specific disk sector. The sector's 128 bytes are displayed in both hexadecimal and ASCII format, greatly easing correction of alphabetic messages.

Both the COPY and DIRECTORY utility programs allow their output to be directed to any specified device. The programmer can perform added file or data verification checks simply by directing these outputs to disk files for subsequent checking. To increase its throughput, the COPY utility also uses double buffering. Along with the Beaver's overlapped I/O this provides extremely fast and efficient performance.

Not so basic Basic

To permit the OEM to realize the power of PETOS, and to provide the OEM with a complete package of easy-to-use software tools, the Beaver is available with a specially designed, ANSI standard extended Basic interpreter which is well equipped to handle almost any scientific or business application. This new Basic permits the programmer to do just about anything that can be done in assembly language. Because the Basic architecture has some unique features which speed execution, this ANSI standard interpreter is one of the fastest on the market.

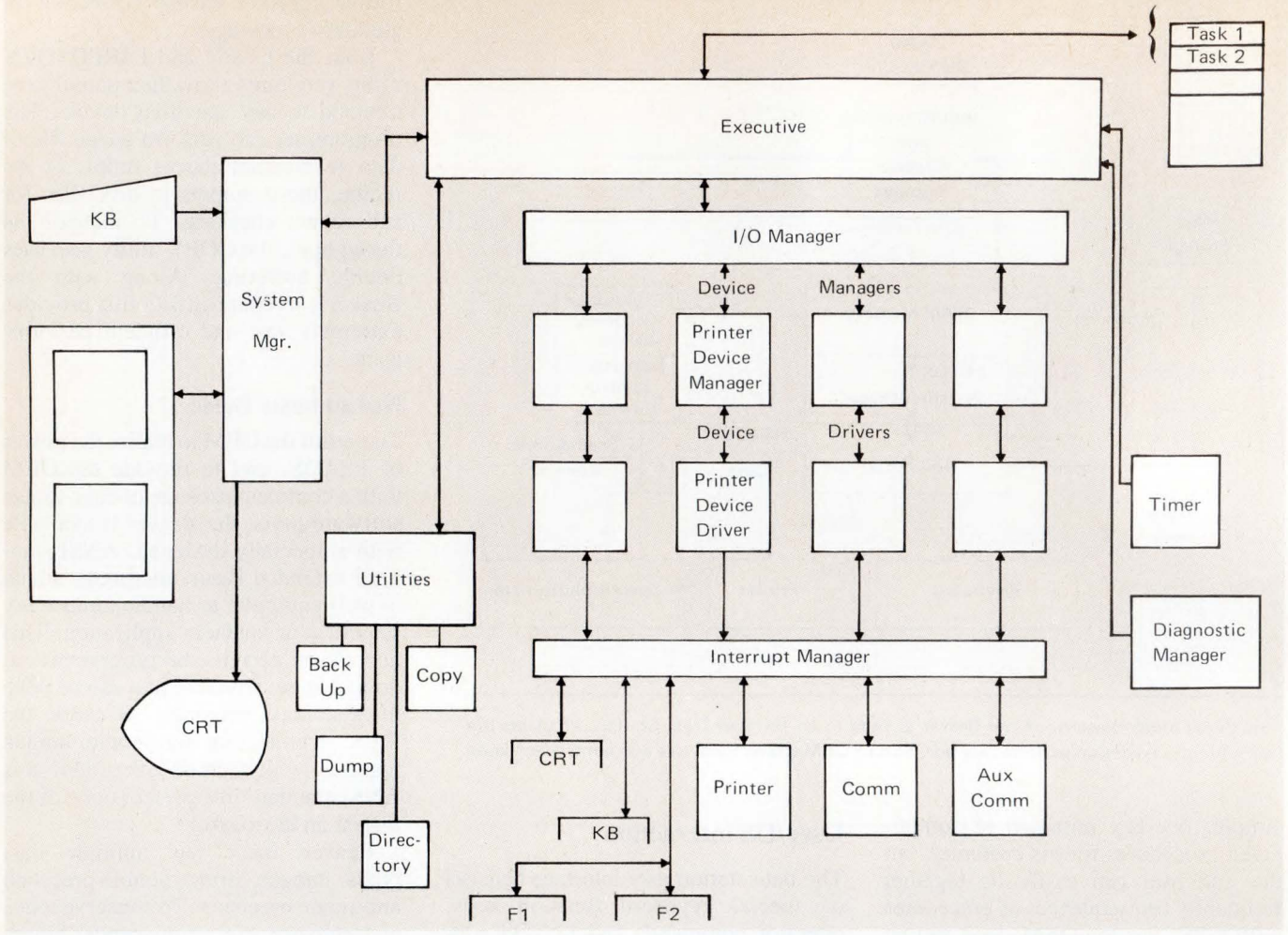
Beaver Basic has multiple data types: integer, string, double precision and single precision. To conserve space and enhance execution speeds, binary is used for all computation and storage. The language has been extended to make it easy to write good programs with features like error trapping, IF. . .THEN. . .ELSE and nested IF. . .THEN. . .ELSE statements, a halt with an error message when division by zero is attempted, no variable name length restraints, built in editor and the ability to use assembler language subroutines.

The wide choice of data formats enables the programmer to choose the one to give him the most speed for his need. Loops and indexing, for example, may be speeded using the integer format.

Basic interpreters generally return to the command mode when an error is encountered. But with error trapping the key operator can be told what was done wrong and given the opportunity to make the correction — thereby avoiding a complicated rerun procedure.

Normally Basics have unformatted output. With the Beaver's PRINT--USING statement the programmer may specify a print format that even includes a floating dollar sign.

Very important to the OEM is the string capability with this interpreter. Usually strings must be allocated ahead



PETOS function diagram. By providing error trapping, the interception of error messages from the system in both BASIC and assembly language application programs, the Beaver permits the programmer to perform necessary remedial action. A pre-determined error routine can be entered to simplify the operator's job, or simply replace the operating system error message with an application-specific message or instruction. Its function is to prevent the need for operator-confusing restarts in the middle of long procedures, which themselves can often produce more errors.

of time but with the data station, variable strings of up to 255 characters can be dynamically allocated. The full complement of string operations includes string search command and the ability to select any number of character from the middle of a string.

The Beaver Basic supports a full set of commands for the disk files as well as having device control over the communications line, printer port and auxiliary port. Three files types are supported: open sequential for input, open sequential for output and random access. Because the data station has device-name independence, any device on the system may be swapped.

Other useful features include data manipulation at the bit level, Boolean functions and multiple statements per line.

Summary

For the OEM designing an intelligent work station around today's intelligent terminals, it can be pure agony making the work station easy-to-use for the end user, if the terminal's software has no built-in provisions with the OEM in mind. The data station is changing this.

Many common, "big systems" features of operating systems such as multitasking, device independence, command substitution systems, multitasking I/O, fixed and variable record modes, I/O request and proceed, system console, sharable system resources, double buffered I/O, interval timers, auxiliary communications interfaces and error trapping, not available in many intelligent terminals designed for the end user market, are now available in intelligent OEM terminals called data stations.

The dichotomy the OEM once faced — to produce a cost-competitive product which at the same time could be readily understood by the non-computer-sophisticated user — is being resolved. No longer must time and effort be wasted, building in needed features.

Recognizing these special OEM needs, Perkin-Elmer recently introduced the first intelligent terminal expressly designed for incorporation into OEM work stations: the Model 3500 Beaver Data Station. This new terminal offers far more flexibility than the typical intelligent terminal — at a lower cost. A look at the Beaver's software capabilities has revealed a rather typical terminal operating system structure. But one having high level software embellishments of particular interest to the OEM — Basic, a macro-assembler, an editor, a good set of utilities and a complete set of communications emulators — all provided to simplify the OEM's development and implementation tasks. DD

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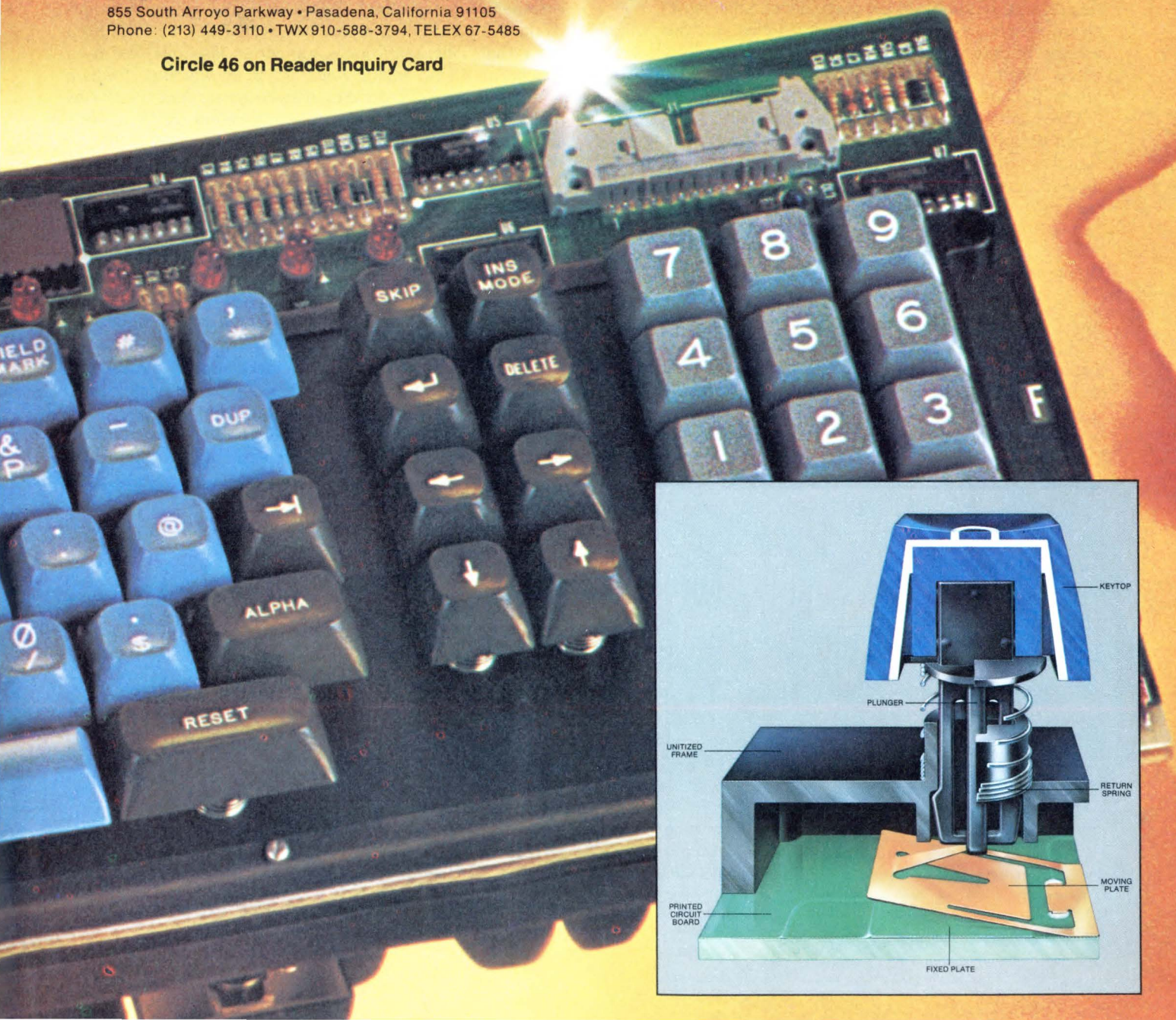


PRINCIPLES OF DATA ACQUISITION AND CONVERSION —Part 1

Eugene L. Zuch
Datel Systems, Inc.

Data acquisition and distribution sytems interface between the real world of physical parameters, which are analog, and the artificial world of digital computation and control. With current emphasis on microcomputer systems, interfacing has become important. In addition, there is the rapid growth in use of microcomputers and minicomputers to perform difficult digital control and measurement functions.

The data converters or A/D-D/A converters (ADC-DAC) which perform the interfacing function between analog and digital worlds are found in data telemetry systems, pulse code modulated communications, automatic test systems, computer display systems, video signal processing systems, data logging systems and sampled-data control systems.

Data conversion: an overview

An amplifier boosts the amplitude of the transducer output signal to a useful level for processing (**Fig 1**). Transducer outputs may be microvolt or millivolt level signals which are then amplified to 1 to 10 volt levels. Furthermore, the transducer output may be a high impedance signal, a differential signal with common-mode noise, a current output, a signal super-imposed on a high voltage, or a combination of these. The amplifier, in order to convert such signals into a high level voltage, may be one of several specialized types.

The amplifier is frequently followed by a low pass active filter which reduces high frequency signal components, unwanted electrical interference noise, or electronic noise from the signal. The amplifier is sometimes also followed by a special nonlinear analog function circuit which performs a nonlinear operation on the high level signal. Such operations include squaring, multimplication, division, RMS conversion, log conversion or linearization.

The processed analog signal next goes to an analog multiplexer which sequentially switches between a number of different analog input channels. Each input is in turn connected to the output of the multiplexer for a specified period of time by the multiplexer switch. During this connection time a S&H circuit acquires the signal voltage and then holds its value while an analog-to-digital converter converts the value into digital form. The resultant digital word goes to a computer data bus or to the input of a digital circuit.

Thus the analog multiplexer, together with the sample-hold, time shares the ADC with a number of analog input channels. The timing and control of the complete data acquisition system is done by a digital circuit called a programmer-sequencer, which in turn is under control of the computer. In

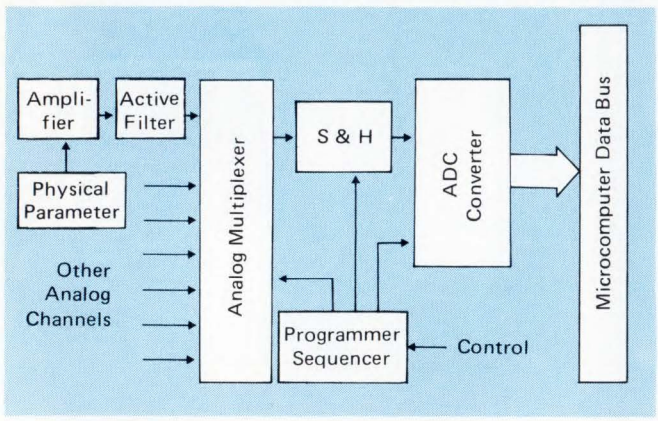


Fig 1. Microcomputerized data acquisition feedback control system shows interconnection of various circuit functions typically found in data acquisition and distribution systems — transducers, amplifiers, filters, nonlinear analog functions, analog multiplexers and sample-holds.

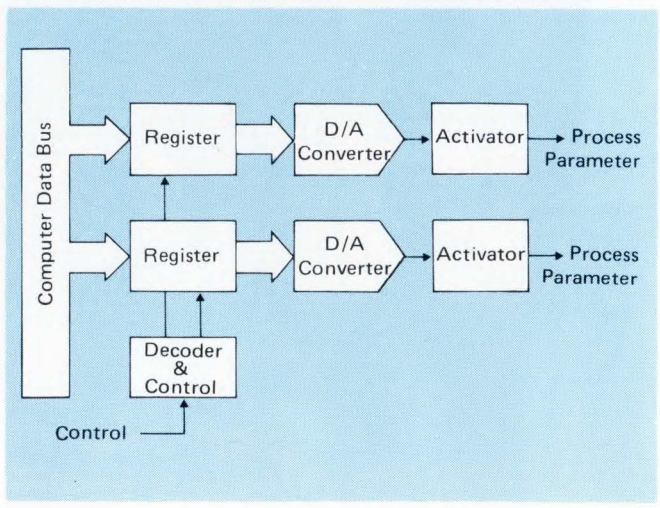


Fig 2. Data distribution system.

Fig 3. Computer-compatible data acquisition and distribution system on a single card.

some cases the computer itself may control the entire data acquistion system.

While this is perhaps the most commonly used data acquisition system configuration, there are alternatives. Instead of multiplexing high-level signals, low-level multiplexing is sometimes used with the amplifier following the multiplexer. In such cases just one amplifier is required, but its gain may have to be changed from one channel to another during multiplexing. Another method is to amplify and convert the signal into digital form at the transducer location and send the digital information in serial form to the computer. Here the digital data must be converted to parallel form and then multiplexed onto the computer data bus. The data distribution portion of a feedback control system, illustrated in **Fig 2**, is the reverse of the data acquisition system. The computer, based on the inputs of the data acquisition system, must close the loop on a process and control it by means of output control functions. These control outputs are in digital form and must therefore be converted into analog form in order to drive the process. The conversion is accomplished by a series of DACs as shown. Each DAC is coupled to the computer data bus by means of a register which stores the digital word until the next update. The registers are activated sequentially by a decoder and control circuit which is under computer control.

The DAC outputs the drive actuators which directly control the various process parameters such as temperature, pressureed by a series of DACs as shown. Each DAC is coupled to the computer data bus by means of a register which stores the digital word until the next update. The registers are actplug-in board which contains a complete data acquisition and distribution system and mates directly with a minicomputer.

Quantizing theory

A/D conversion in its basic conceptual form can be thought of as a two-step process — quantizing and coding. Quantizing is the process of transforming a continuous analog signal into a set of discrete output states. Coding is the process of assigning a digital code word to each of the output states. Some of the early ADCs were appropriately called quantizing encoders.

The nonlinear transfer function shown in **Fig4** is that of an ideal quantizer with 8 output states; with output code words assigned, it is also that of a 3-bit ADC. The 8 output states are assigned the sequence of binary numbers from 000 through 111. The analog input range for this quantizer is 0 to +10V. There are early ADCs were appropriately called quantizing encoders.

There are several important points concerning the transfer function of **Fig 4**. First, the resolution of the quantizer is defined as the number of output states expressed in bits; in this case it is a 3-bit quantizer. The number of output states for a binary coded quantizer is 2n, where n is the number of bits. Thus, an 8-bit quantizer has 256 output states and a 12-bit quantizer has 4096 output states.

As shown in the diagram, there are 2^n-1 analog decision points (or threshold levels) in the transfer function. These points are at voltages of +0.625, +1.875, +3.125, +4.375, +5.625, +6.875 and +8.125. The decision points must be precisely set in a quantizer in order to divide the analog voltage range into the correct quantized values.

The voltages +1.25, +2.50, +3.75, +5.00, +6.25, +7.50, and +8.75 are the center points of each output code word. The analog decision point voltages are precisely halfway between the code word center points. The quantizer staircase function is the best approximation which can be made to a straight line drawn through the origin and full scale point, notice that the line passes through all of the code word center points.

At any part of the in+8.75 are the center points of each output code word. The analog decision point voltages are precisely halfway between the code word center points. The quantizer staircase function jacent decision points and is known as the analog quantization size, or quantum, Q. In **Fig 4**, the quantum is 1.25V and is found in general by dividing the full scale analog range by the number of output states. Thus: $Q=FSR/2^n$.

FSR is the full scale range which is 10V in this case. Q is the smallest analog difference which can be resolved, or distinguished, by the quantizer. In the case of a 12-bit quantizer, the quantum is much smaller and is found to be: $Q=FSR/2^n$

or $Q=10V/4096$

or $Q=2.44mV$.

If the quantizer input is moved through its entire range of analog values and the difference between output and input is taken, a sawtooth error function results, as shown in **Fig 4.** This function is called the quantizing error and is the irreducible error which results from the quantizing process. It can be reduced only by increasing the number of output states (or the resolution) of the quantizer, thereby making the quantization finer.

Sawtooth error function

For a given analog input value to the quantizer, the output and input is taken, a sawtooth error function results, as shown in **Fig 4**. This function is called the quantizing error and is the irreducible error which resultsantization uncertainty or quantization noise. The quantizer output can be thought of as the analog input with quantization noise added to it. The noise has a peak-to-peak value of Q but, as with other types of noise, the average value is zero. Its RMS value, however, is useful in analysis and can be computed from the triangular waveshape to be $Q/2\sqrt{3}$.

western peripherals

GENERAL PRODUCT DESCRIPTION

MAGNETIC TAPE AND DISC CONTROL SYSTEMS

Western Peripherals controllers for ½" magnetic tape, ¼" data cartridge tape, fixed and removable cartridge discs, and storage module discs for mini- and microcomputers offer the most advanced features by utilizing the latest in solid state microcircuit technology. These embedded controllers are designed to mount totally within the host computer. This insures uniform electrical and physical environmental conditions while saving the cost of non-essential cabinetry.

INDIVIDUAL CONTROLLERS OR COMPLETE SYSTEMS

Western Peripherals' controllers are sold separately, or as complete systems integrated and tested with a selected drive (or drives), and installed in the customer's computer. Both individual controllers and complete systems are covered by Western Peripherals' one-year factory warranty.

STORAGE MODULE DISC CONTROLLER

NEW

DC-233 FOR DIGITAL EQUIPMENT CORPORATION PDP-11 COMPUTERS

The DC-233 is designed to accommodate up to eight of the large capacity non-removable and removable media multiplatter disc drives in the range of 50 to 300 megabytes.

When used with the CDC 9762 80 megabyte drive, the DC-233 emulates and is media-compatible with the DEC RM03 with a formatted capacity of 67 megabytes per drive. When used with the Memorex 677 series 100/200 megabyte drives, the DC-233 emulates the DEC RPO5/RPO6 systems with 88 or 176 megabytes per drive.

The DC-233 is an embedded controller based upon a microprocessor employing bit slice technology. Like the DEC RMO3 disc system, the DC-233 consists of a high speed controller and from one to eight drive adapters. However, unlike the RMO3 system, both the controller and adapters are housed together within the CPU or expansion chassis. Since each drive has its own adapter, and cabling, it is a true radial configuration, thus effectively isolating one drive from another. Each drive adapter has within it a microprocessor whose function is to control the commands and status associated with its drive. The controller portion with its own microprocessor handles all communications to the CPU and implements the data transfers as well as the error correction coding and decoding.

This controller/adapter arrangement means that the DC-233 stays software-compatible no matter how many drives are being used since each drive and adapter can communicate status and command information with the CPU while any other drive is transferring data.

The data transfer section is throttled automatically, dependent upon the NPR demand of other devices and the data rate of the drive. Dual drive porting is totally supported for all drives having that capability. Dual unibus porting is also an available option.

FEATURES

- Software compatible to all DEC operating systems having RMO3 or RPO5/RPO6 support.
- Media compatible.
- Completely imbedded.
- Radial cabling configuration.
- Microprocessor based.
- ECC fully implemented.
- All local as well as remote registers fully implemented.
- Automatic NPR throttling.

Circle 109 on Reader Inquiry Card

Control Data Corp. 9762 Storage Module

Memorex 677 Disk Storage Drive

UNIVERSAL MAGNETIC TAPE CONTROLLERS

TC-120 FOR DATA GENERAL AND D.G. EMULATING COMPUTERS

The TC-120 Magnetic Tape Controller combines both PE and NRZ formats on one board to fit all NOVA, Eclipse, and other Data General emulating computers. It provides the ability to mix 7-track and 9-track NRZ, PE, or dual-density tape units in any combination up to eight drives at any two speeds in the range of 12.5 to 125 ips.

On 7-track, its 4-6-6 pack allows the user to dump core memory onto tape; and a 33-word data buffer, instead of the usual 2-word buffer, gives greater flexibility in assigning DMA priorities in the computer.

Read-and-write on the fly, another special feature, allows automatic non-stop operation when doing consecutive read-write operations, and it saves switching time when switching between multiple tape units. This is accomplished automatically without special software or software restrictions.

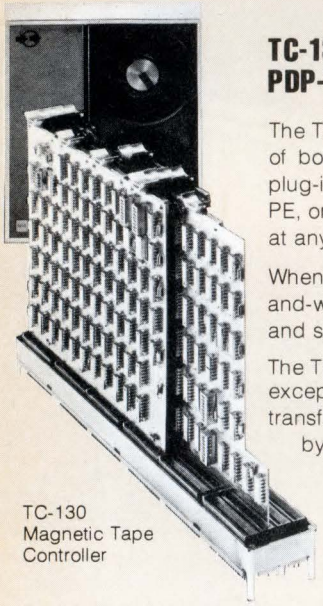
Data General Compatible

The TC-120 is software compatible with all Data General NOVA and Eclipse series computers and other Data General emulating computers. Virtually any tape drive having an industry standard interface can be used with the TC-120.

FEATURES

- Dual speed capability.
- IRIS and RDOS compatible.
- IBM 360 compatible format in both PE and NRZ.
- Read after write parity check.
- 33-word data buffer.
- Two or three byte 7-track packing (software controlled).
- On-the-fly operation for consecutive reads or writes.
- Allows user to edit previously recorded records.
- Comprehensive diagnostic programs provided.
- Tape drive connections are via a push-on connector to the CPU backplane.
- Single board embedded.

Circle 110 on Reader Inquiry Card



TC-130
Magnetic Tape
Controller

TC-130 FOR DIGITAL EQUIPMENT CORPORATION PDP-11 COMPUTERS

The TC-130 Magnetic Tape Controller offers users the convenience of both Phase Encode and NRZ formats consolidated onto four plug-in PC boards. It also has the ability to mix 7- and 9-track NRZ, PE, or dual-density tape units in any combination up to eight drives at any two speeds in the range of 12.5 to 125 ips.

When doing consecutive read-write operations, the TC-130's read-and-write on the fly capability permits automatic non-stop operation, and saves time when switching between multiple tape units.

The TC-130's logic does all data transfers in the word (16 bit) mode except for odd bytes at the beginning or end of a block. These are transferred in the byte (8 bit) mode, thus reducing data transfers by almost 50% compared to other systems. The TC-130 also has a 33-word data buffer instead of the usual two-byte buffer. This allows greater flexibility in assigning priorities within the computer.

DEC PDP-11 (TM11) Compatible

The TC-130 is software and hardware compatible with all PDP-11 series computers. Virtually all tape drives having an industry standard interface can be used with the TC-130. These include drives from Ampex, Cipher, Kennedy, Pertec, Qantex, STC, Tandberg, Telex and Wangco.

FEATURES

- Word transfer of data used where byte transfer is not necessary.
- DEC or IBM byte packing under software control.
- IBM 360 compatible format in both NRZ and PE.
- 33-word data buffer.
- Handles up to eight tape drives.
- Allows user to edit previously recorded data.
- Dual speed capability.
- Comprehensive diagnostics.
- Software compatible (TM 11).
- Embedded — The TC-130 resides within the host CPU.
- Fits all PDP-11 series computers.
- Permits automatic read-and-write on the fly for consecutive read-write operations.

Circle 111 on Reader Inquiry Card

TC-140 FOR INTERDATA SERIES COMPUTERS

The TC-140 Magnetic Tape Controller combines both PE and NRZ formats on one board to fit Interdata computers. It provides the ability to mix 7-track and 9-track NRZ, PE, or dual-density tape units in any combination up to four drives at any two speeds in the range of 12.5 to 125 ips.

Its device code is switch-settable on the controller, allowing multiple controllers in one CPU each with up to four drives.

The TC-140's enhanced command set and extended status register (which remain "invisible" under standard operating systems) allow a higher level of control for special applications.

The TC-140 is software compatible to all Interdata operating systems having magnetic tape support and runs through either the multiplexer bus or SELCH.

FEATURES

- Interdata software compatible.
- Single-board, embedded, provides both PE and NRZ formats.
- Allows mixing 7-track or 9-track, PE, NRZ, or dual-density tape units in any combination.
- Provides 4 × 4 or 6-bit pack on 7-track for dumping core memory onto tape.
- 66-byte data buffer increases flexibility in assigning priorities when programming data transfer.
- IBM 360 compatible 7/9 channel format.
- Operates via SELCH or multiplexer bus.
- Comprehensive diagnostic program.
- Enhanced command and extended status set.

Circle 112 on Reader Inquiry Card

TC-150 FOR DIGITAL EQUIPMENT CORPORATION LSI-11 COMPUTERS

The TC-150 Magnetic Tape Controller offers users the convenience of both Phase Encode and NRZ formats consolidated onto four plug-in PC boards. It also has the ability to mix 7- and 9-track NRZ, PE, or dual-density tape units in any combination up to eight drives at any two speeds in the range of 12.5 to 125 ips.

When doing consecutive read-write operations, the TC-150 read-and-write on the fly capability permits automatic non-stop operation, and saves time when switching between multiple tape units.

The TC-150 logic does all data transfers in the word (16 bit) mode except for odd bytes at the beginning or end of a block. These are transferred in the byte (8 bit) mode, thus reducing data transfers by almost 50% compared to other systems. The TC-150 also has a 33-word data buffer instead of the usual two-byte buffer. This allows greater flexibility in assigning priorities within the computer.

DEC LSI-11 compatible

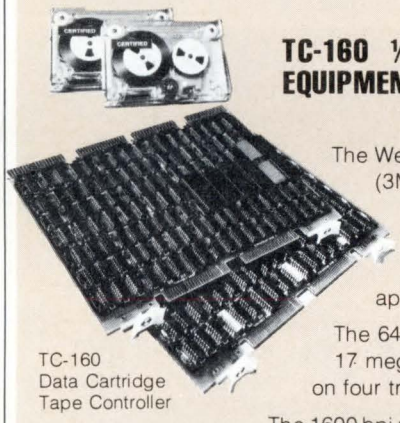
The TC-150 is software and hardware compatible with all LSI-11 Series computers. Virtually all tape drives having an industry standard interface can be used with the TC-150.

FEATURES

- Word transfer of data used where byte transfer is not necessary.
- DEC or IBM byte packing under software control.
- IBM 360 compatible format, in both NRZ and PE.
- 33-word data buffer.
- Handles up to eight tape drives.
- Allows user to edit previously recorded data.
- 7-track 4 × 4 or 2 × 6 packing.
- Dual speed capability.
- Q bus buffer provided to isolate the TC-150 and its associated cabling from the bus.
- Embedded.
- Software compatible (TM 11).

Circle 113 on Reader Inquiry Card

DATA CARTRIDGE TAPE CONTROLLERS



TC-160
Data Cartridge
Tape Controller

TC-160 ¼" DATA CARTRIDGE TAPE CONTROLLER FOR DIGITAL EQUIPMENT CORPORATION LSI-11 COMPUTERS

The Western Peripherals TC-160 Controller for ¼" Data Cartridge (3M type) drives offers users the convenience of handling ease and compact size inherent in this style of drive.

Built-in Tri-mode formatting of the TC-160 allows the user to select the drive type and format best suited to his application.

The 6400 bpi MFM formatting offers unformatted capacities up to 17 megabyte on a single DC-450 (450') cartridge. Data is written on four tracks in serial mode.

The 1600 bpi phase encode four-track parallel format allows the full tape to be written or read in a single pass with up to 4 megabytes of data on a single cartridge.

The 1600 bpi phase encode four-track serial also has a total storage capacity of 4 megabytes. Sixteen-word write and read data buffers are used in the TC-160 instead of the usual two-bytes, giving greater flexibility in assigning priorities on the computer.

The TC-160 is hardware compatible with all LSI-11 series computers. The two controller boards plug directly into the computer Q bus. The TC-160 is software compatible to all operating systems or utilities having DEC TM 11/TU 10 support.

NEW

FEATURES

- Emulates DEC TM 11/TU 10 ½" magnetic tape system.
- Embedded — two quad controller cards plug into any two adjacent DEC Q bus slots with no special wiring required.
- Controls up to eight drives.
- Any of three formats: 6400 bpi serial MFM, 1600 bpi PE serial, or 1600 bpi PE parallel.
- 16-byte data buffer eases DEC Q bus priority positioning.

Circle 114 on Reader Inquiry Card

TC-170 ¼" DATA CARTRIDGE TAPE CONTROLLER FOR DATA GENERAL NOVA COMPUTERS AND EMULATORS

The Western Peripherals TC-170 Controller for ¼" Data Cartridge (3M type) drives offers users the convenience of handling ease and compact size inherent in this style of drive.

Built-in tri-mode formatting of the TC-170 allows the user to select the drive type and format best suited to his application.

The 6400 bpi MFM formatting offers unformatted capacities up to 17 megabyte on a single DC-450 (450') cartridge. Data is written on four tracks in serial mode.

The 1600 bpi phase encode four-track parallel format allows the full tape to be written or read in a single pass with up to 4 megabyte of data on a single DC-450 cartridge.

The 1600 bpi phase encode four-track serial also has a total storage capacity of 4 megabyte. Write and read data buffers are used in the TC-170, giving greater flexibility in assigning priorities on the computer.

The TC-170 is hardware and software compatible with all Data General NOVA and Eclipse Series, as well as other Data General emulating computers. The embedded controller plugs into a single slot in the host computer and connects with the tape drive through the backplane of the computer, using push-on connectors.

NEW

FEATURES

- Emulates D.G. 6020/4196 ½" Magnetic Tape System.
- Embedded — single board controller plugs into any slot.
- Controls up to eight drives.
- Any of three formats: 6400 bpi serial MFM, 1600 bpi PE serial, or 1600 bpi PE parallel.
- 16-byte data buffer eases priority positioning.

Circle 115 on Reader Inquiry Card

UNIVERSAL DISC CONTROLLERS

DC-220 FOR DATA GENERAL NOVA COMPUTERS

The DC-220A Series Disc Controllers operate with all Data General NOVA and Eclipse computers as well as other Data General-emulators. DC-220's are available in three configurations compatible with the Data General 4057, 4234, and 4047 systems. All versions are mounted on single PC boards to occupy a single card slot inside the computer.

DC-220A-25 Multi-surface Drive Controller Emulates the Data General 4057 System

☐ RDOS compatible ☐ Maximum capacity 100 megabytes using four 25-megabyte drives such as the Calcomp 114; or two 50-megabyte drives such as the CDC 9746 or Calcomp 214; or one 100-megabyte drive such as the Calcomp 215.

DC-220A-10 Cartridge Drive Controller Emulates the Data General 4234 System

☐ RDOS compatible ☐ Data General media compatible using 5440-type drives ☐ Also available with 2315-type drives ☐ Maximum capacity 40 megabytes using four 10-megabyte drives or two 20-megabyte drives.

DC-220A-2.5 Cartridge Drive Controller Emulates the Data General 4047 System

☐ RDOS compatible ☐ Data General media compatible using 2315-type drives ☐ Also available with 5440-type drives ☐ Maximum capacity 10 megabytes using four 2.5-megabyte drives, two 5-megabyte drives, or one 10-megabyte drive.

FEATURES

- Lets computer see multi-disc platters as though from separate drives.
- Stores track associated with every computer-selected drive even if there is in reality only one drive mechanism.
- Performs automatic seek as part of read-write operation.
- Compatible with Data General RDOS software.
- Complete data error checking.
- Choice of formats with or without address verification.
- Simplified system installation, maintenance, and service.
- Electrical connection to the drive via push-on connections to the CPU backplane.
- Switch selectable implied seek on read.
- Single board embedded.

Circle 116 on Reader Inquiry Card

DC-230 FOR DIGITAL EQUIPMENT CORPORATION PDP-11 COMPUTERS

The DC-230 Disc Controller is designed to accommodate both dual-platter and single-platter drives with 203 or 406 tracks per surface.

Because the controller stores the track information associated with present selected drive, the seek operation need not be issued separately. The operator simply issues a new disc address for the drive stipulating the desired track. The seek operation then occurs automatically when the operator activates the read-write command with a "go" pulse.

Cartridge Drive Control

☐ Capable of controlling eight 2.5-megabyte drives, four 5-megabyte drives, two 10-megabyte drives, or one 20-megabyte drive. The standard DC-230 interfaces with almost any desired cartridge drive while retaining total software compatibility to the DEC RK11/RKO5 system.

The data on the 2315 cartridge (at 100 TP) is also media compatible with DEC.

The DC-230 is software compatible with the PDP-11. The two controller boards plug into two slots in the computer or expansion chassis and connect with the disc drive from connectors coming off the top of one of the boards.

FEATURES

- Lets computer see multi-disc platter drives as though from separate drives.
- Performs automatic seek as part of read-write operation.
- Complete data error checking.
- Fits all PDP-11 computers.
- Simplified system installation, maintenance, and service.
- Up to 20 megabytes total storage.
- PDP-11 software compatible.
- 16-bit word data buffer.
- RK11 software compatible.
- Two board embedded.

Circle 117 on Reader Inquiry Card

GENERAL INFORMATION

DIAGNOSTIC PROGRAM

Comprehensive diagnostic programs are supplied with all control systems for testing the Western Peripherals Magnetic Tape or Disc Controller, and insuring compatibility with the standard operating system under dynamic operating conditions.

ORDERING INFORMATION

All sales are FOB Anaheim, California. Payment terms are Net 30 days subject to credit approval. Specifications listed are subject to change without notice.

SERVICE

Western Peripherals' combination of nationwide contract service and worldwide Distributor service network assures you of support at almost any point on the globe. Customer training is available at the Western Peripherals plant for both controllers and drives. It is provided at a nominal cost for material and supplies or can be quoted at the customer's site.

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Linthicum, MD 21090
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Lewisville, Texas 75067
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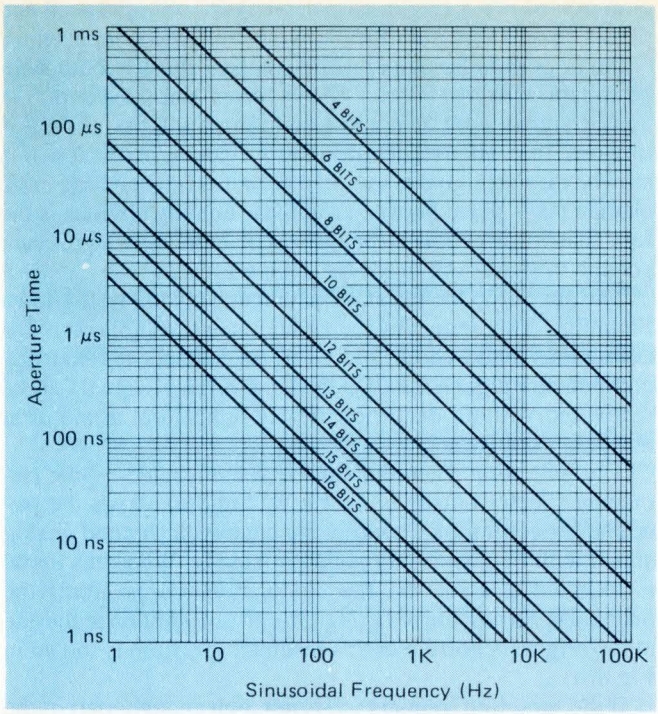

Fig 4. Transfer function of ideal 3-bit quantizer.

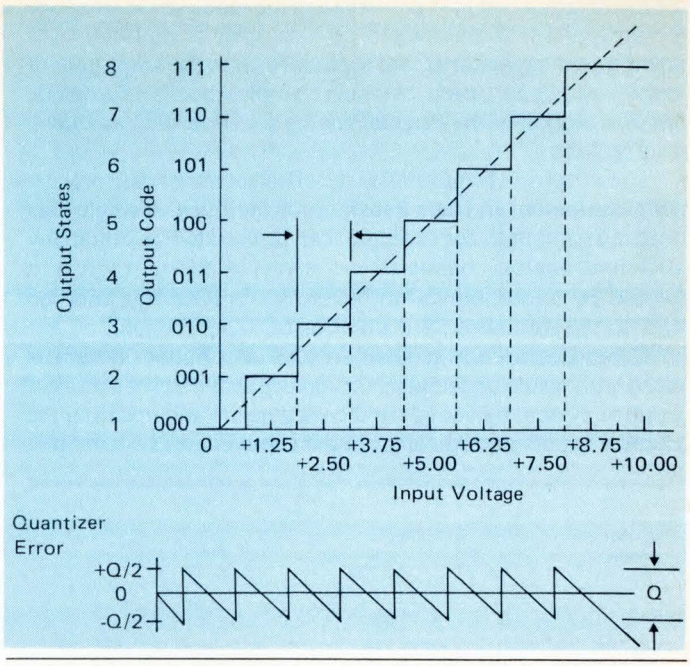

Fig 6. Graph for aperture error for sinusoidal signals.

Sampling theory

An ADC requires a small, but significant, amount of time to perform the quantizing and coding operations. The time required to make the conversion depends on several factors: the converter resolution, the conversion technique, and the speed of the components employed in the converter. The conversion speed required for a particular application depends on the time variation of the signal to be converted and on the accuracy desired.

Conversion time is frequently referred to as aperture time. In general, aperture time refers to the time uncertainty (or time window) in making a measurement and results in an amplitude uncertainty (or error) in the measurement if the signal is changing during this time.

As shown in **Fig 5,** the input signal to the ADC changes by ΔV during the aperture time t_a in which the conversion is performed. The error can be considered an amplitude error or a time error; the two are related as follows: $\Delta V = t_a\,(dV(t)/dt)$ where $dV(t)/dt$ is the rate of change with time of the input signal.

Note that ΔV represents maximum error due to signal change, since actual error depends on how the conversion is done. At some point in time within t, signal amplitude corresponds exactly with the output code word produced.

For the specific case of a sinusoidal input signal, the maximum rate of change occurs at the waveforms zero crossing, and amplitude error is: $\Delta V = t_a\ d@(A\sin\omega t)\ t{=}o]/dt{=}t_aA\omega$.

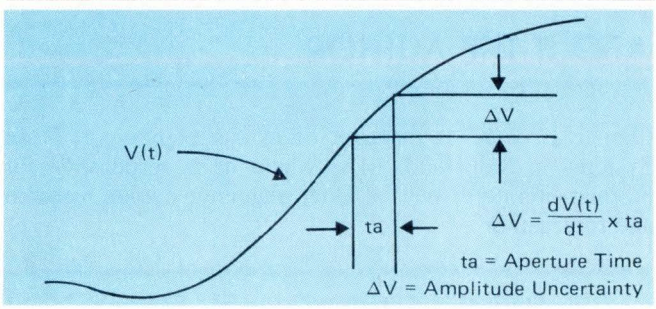

Fig 5. Aperture time and amplitude uncertainty.

The resultant error as a fraction of the peak to peak full scale value is: $\epsilon = \Delta V/(2A) = \pi f t_a$. From this result the aperture time required to digitize a 1kHz rate of change occurs at the waveforms zero crossing, and amplitude error is: $\Delta V = t_a\ d@(A\sin\omega t)\ t{=}o]/dt{=}t_aA\omega$.

The resultant error as a fraction of the peak to peak full scale value is: $\epsilon = \Delta V/(2A) = \pi f t_a$. From this result the aperture time required to digitize a 1kHz signal to 10 bits resolution can be found. The resolution required is one part in 2^{10} or 0.001. So: $t_a = \epsilon/(\pi f) = 0.001/3.14\times10^3 = 320\times10^{-9}$.

The result is a required aperture time of just 320 nsec! One should appreciate the fact that 1 KHz is not a particularly fast signal, yet it is difficult to find a 10-bit ADC to perform this conversion at any price! Fortunately, there is a relatively simple and inexpensive way around this dilemma by using an S&H circuit.

An S&H circuit samples the signal voltage and then stores it on a capacitor for the time required to perform the A/D conversion. The aperture time of the ADC is therefore greatly reduced by the much shorter aperture time of the S&H circuit. In turn, the aperture time of the S&H is a function of its bandwidth and switching time.

Fig 6 is a useful graph which is the result of Equation 5. It gives the aperture time required for converting sinusoidal signals to a maximum error less than one part in 2^n where n is the resolution of the converter in bits. The peak to peak value of the sinusoid is assumed to be the full scale range of the ADC. The graph is most useful in selecting a S&H by aperture time or an ADC by conversion time.

In data acquisition and distribution systems, and other sampled-data systems, analog signals are sampled on a periodic basis as illustrated in **Fig 7**. The train of sampling pulses in **7(b)** represents a fast-acting switch which connects to the analog signal for a very short time and then disconnects for the remainder of the sampling period. The result of the fast-acting sampler is identical with multiplying the analog signal by a train of sampling pulses of unity amplitude, giving the modulated pulse train of **Fig 7(c).** The amplitude

of the original signal is preserved in the modulation envelope of the pulses. If the switch type sampler is replaced by a switch and capacitor (a S&H circuit), then the amplitude of each sample is stored between samples and a reasonable reconstruction of the original analog signal results, as shown in **Fig 7(d).**

The purpose of sampling is the efficient use of data processing equipment and data transmission facilities. A single data transmission link, for example, can be used to transmit many different analog channels on a sampled basis, whereas it would be uneconomical to devote a complete transmission link to the continuous transmission of a single signal.

Likewise, a data acquisition and distribution system is used to measure and control the many parameters of a process control system by sampling the parameters and updating the control inputs periodically. In data conversion systems it is common to use a single, expensive ADC of high speed and precision and then multiplex a number of analog inputs to it.

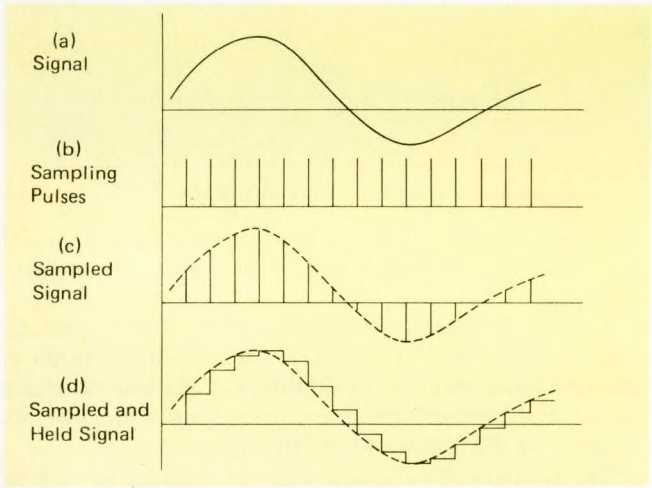

Fig 7. Signal sampling.

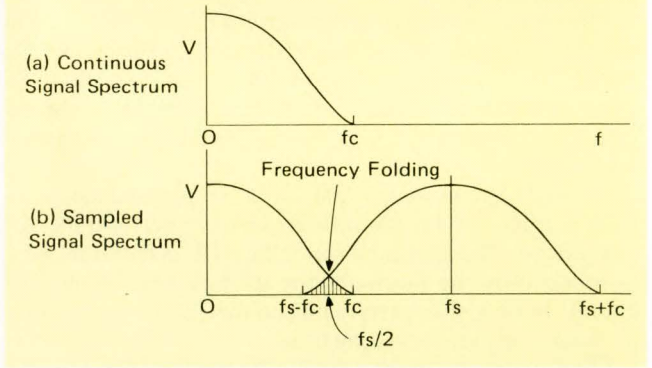

Fig 8. Frequency spectra demonstrating the sampling theorem.

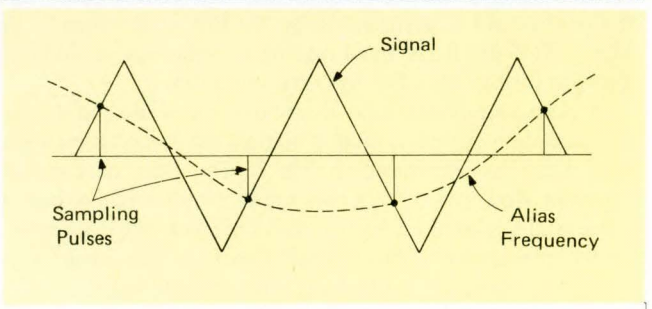

Fig 9. Alias frequency caused by inadequate sampling rate.

An important fundamental question to answer about sampled-data systems is this: "How often must I sample an analog signal in order not to lose information from it?" It is obvious that all useful information can be extracted if a slowly varying signal is sampled at a rate such that little or no change takes place between samples. Equally obvious is the fact that information is being lost if there is a significant change in signal amplitude between samples.

The answer to the question is contained in the well-known Sampling Theorem which may be stated as follows: If a continuous, band-width-limited signal contains no frequency components higher than f_c, then the original signal can be recovered without distortion if it is sampled at a rate of at least $2f_c$ samples/sec.

The Sampling Theorem can be demonstrated by the frequency spectra illustrated in **Fig 8**. **Fig 8(a)** shows the frequency spectrum of a continuous bandwidth-limited analog signal with frequency components out to f_c. When this signal is sampled at a rate f_s, the modulation process shifts the original spectrum out to f_s, $2f_s$, $3f_s$, etc. in addition to the one at the origin. A portion of this resultant spectrum is shown in **Fig 8(b)**.

If the sampling frequency f_s is not high enough, part of the spectrum centered about f_s will fold over into the original signal spectrum. This undesirable effect is called frequency folding. In the process of recovering the original signal, the folded part of the spectrum causes distortion in the recovered signal and cannot be eliminated by filtering the recovered signal. From the figure, if the sampling rate is increased such that $f_s - f_c > f_c$, then the two spectra are separated and the original signal can be recovered without distortion. This demonstrates the result of the Sampling Theorem that $f_s \geq 2f_c$. Frequency folding can be eliminated in two ways: first by using a high enough sampling rate, and second by filtering the signal before sampling to limit its bandwidth to $f_s/2$.

One must appreciate the fact that in practice there is always some frequency folding present due to high frequency signal components, noise, and nonideal presample filtering. The effect must be reduced to negligible amounts for the particular application by using a sufficiently high sampling rate. The required rate, in fact, may be much higher than the minimum indicated by the Sampling Theorem.

The effect of an inadequate sampling rate on a sinusoid is illustrated in **Fig 9;** an alias frequency in the recovered signal results. In this case, sampling at a rate slightly less than twice per cycle gives the low frequency sinusoid shown by the dotted line in the recovered signal. The alias frequency can be significantly different from the original frequency. From the figure it is easy to see that if the sinusoid is sampled at least twice per cycle, as required by the Sampling Theorem, the original frequency is preserved. DD

ABOUT THE AUTHOR

Eugene L. Zuch is manager of market planning at Datel Systems in Mansfield, MA, where he is responsible for product literature, new product planning, market research and forecasting.

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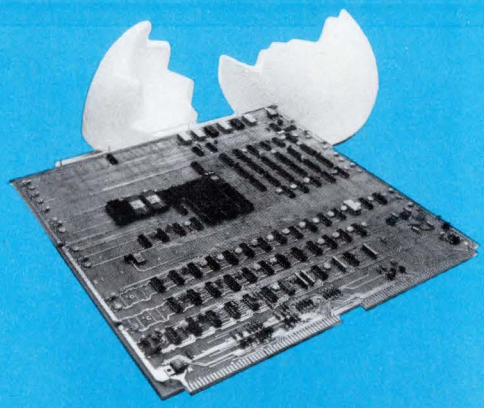

MODEL 2310

MODEL 2603

MODEL 2001

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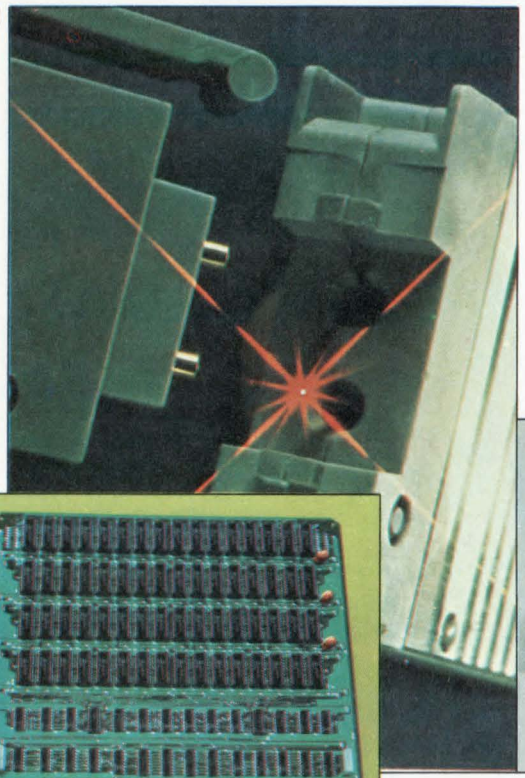
1



1979 National Computer Conference

2

3

NCC '79

THE COMPLETE COMPUTING EXPERIENCE

4

1 Data Communications
2 Computers
3 Memories
4 Peripherals

The latest trends in the use of computers in business and professional applications will highlight the 1979 National Computer Conference, June 4-7 in New York City. The technical and professional program, combined with a record-breaking exhibition, will make NCC '79 a conference of enormous scope and diversity. . .truly the world's largest computer show to date.

More than 150 program sessions will cover applications, science and technology, management, and social implications. Emphasis will be on practical solutions to data processing problems. All sessions fit into four basic categories — applications, science and technology, management, and social implications. A special feature will be three separate groups of sessions on the use of computers for financial transactions, in law and public policy, and in health care.

HIGHLIGHTS

- The world's most comprehensive computer conference, June 4-7 in New York City.
- The year's largest exhibit of computer products and services occupying approximately 1,500 booths on all four floors of the New York Coliseum.
- 150 program session emphasizing the four major areas of management, applications, science and technology, and social implications.
- A Personal Computing Festival of commercial exhibits, application demonstrations, and technical sessions on microcomputer systems and applications.
- A series of Professional Development Seminars on topics critical to professional growth and advancement.
- A wide range of special events . . . including Pioneer Day, featured addresses, the all-conference reception, and leisure-time activities.
- The NCC'79 Travel Service, offering the most economical travel packages tailored to individual needs.
- Advance NCC registration . . . providing full-conference preregistrants with special discounts and other benefits.

World's largest show

NCC '79 will break all previous records for data processing exhibitions. Exhibits will occupy more than 1,700 booths on all four floors at the New York Coliseum and on the second floor of the New York Hilton Hotel. Products and services displayed will include micros and minis, memory systems, terminals and other peripherals, software systems, data communications equipment, work processing systems, computer leasing services and much more.

The latest computer hardware, systems, and services will be on display on all four floors of the New York Coliseum and at the nearby New York Hilton Hotel. More than 350 organizations will occupy nearly 1,700 booths, making this the largest exhibit of its kind ever assembled. To enhance personal, managerial and technical growth, NCC '79 will feature 16 one-day Professional Development Seminars in the New York Sheraton Hotel designed to enhance professional skills and aid in career development. Specific topics range from database machines, implementing a word processing system, and computer systems performance to structured systems design, an introduction to microprocessors and human engineering in teleprocessing systems.

Underscoring the stature of NCC '79 will be a variety of featured events beginning with the keynote address by John R. Opel, president of IBM. Mr. Opel is a member of the IBM Corporate Office, serves on the board of directors, and formerly was group executive of the Data Processing Product Group.

The NCC '79 sessions, panels, tutorials and special briefings bring you up-to-date on issues, technological developments and applications affecting the computer field. Included in this far-ranging program will be three separate groups of sessions covering management concerns, privacy and security, and social issues.

Management briefings will cover areas of concern to corporate executives, DP managers and computer specialists. Topics will cover unions and data processing, end user training, why managers fail, improving performance of DP personnel and effective management of data processing projects.

Other sessions tell how to sell new technology to management, determine the value of computer applications, the expanding world of service, computer center management by contract and finding the value of used computers. Rounding out this high-interest area will be additional sessions including several on computers for the chief executive plus an in depth examination of time management.

The problems of computer security and privacy will be addressed by leading authorities, technologists, and practitioners in ten sessions organized by Robert P. Campbell, Department of the Army, Washington, DC. Both managerial and technological aspects will be covered with emphasis on innovative alternatives now available and anticipated new technological developments. Included will be sessions on managing computer security systems, and need for detection and prosecution of abusers.

Social issues in computing, organized by Carol P. Landis of EDUCOM, Princeton, NJ, will cover topics ranging from human factors in computer conferencing to the impact of MIS and other computer-based systems on the organization. Studies by the Minnesota Educational Computing consortium and the Association for Computing Machinery will be analyzed at a session on computer literacy. The impact of computers on the corporate enterprise will be explored in a session covering recent research findings and how these can aid in development of more successful computing systems.

Personal computing

Personal computing has grown beyond the dedicated amateur to create new challenges and opportunities for the computer professional. The NCC '79 Personal Computing Festival, also June 4-7 in the Sheraton Centre Hotel (formerly the Americana) will provide a full program of over 25 technical sessions, demonstrations and commercial exhibits.

Participants will examine the growing role of microcomputers in such areas as the hobby shop, the playroom, the kitchen, the sickroom and the office. Festival sessions will focus on applications of microcomputer techno-

logy in a variety of areas including personal computers as an aid to the handicapped and chronically ill, as a tool in one's hobby or profession, in community service, and in personal investment analysis.

Additional program topics will range from investment analysis and computer music to inter-computer communications and small business systems. And at the festival exhibit program you'll see the latest in personal computing products and services, including such offerings as microprocessors, microcomputers, microprinters, speech synthesizers, floppy disks, cassettes, software packages and database query systems.

New this year will be awards for the best papers accepted for publication in the "Personal Computing Proceedings". Valuable prizes, contributed by NCC exhibitors, will be awarded at the festival for top papers in several subject areas and for outstanding live demonstrations.

Special activities

You'll find a host of special events and activities waiting for you — an all-conference reception, a Science Film Theatre, a series of contests and application demonstrations in personal computing and a Pioneer Day Program. And all this plus Manhattan, the center of the business and financial community and the world's cultural and entertainment capital.

A Computer Philatelic Exhibit, organized with the cooperation of the Computer Study Unit of the American Topical Association, will be featured at the New York Hilton Hotel. Collectors and organizations submitted computer-related exhibits. Prizes will be awarded for the best individual exhibits and, as a service to attendees, cacheted envelopes and covers will be serviced using a special NCC cancellation at a temporary postal substation at the New York Coliseum.

Pioneer Day at NCC '79 will honor a milestone in the history of computing — the development of COBOL. During the 20 years since initial planning began for development of COBOL, this programming language has become the most widely used in the world. The Pioneer Day Program under the direction of Henry P. Stevenson, programming supervisor at the Analytical Support Center of AT&T in Basking Ridge, NJ, will include a special session on COBOL featuring participation of pioneers who played a critical role in its inception and development.

In addition to conference activities, New York City offers attractions for every taste. If demand is sufficient, the NCC '79 Steering Committee will arrange for special leisure activities in the Big Apple — theatre and concert tickets, tours, sightseeing, boat rides, or special visits to museums or other historical and cultural landmarks.

Registration

Those who already preregistered (May 15 deadline) are insured fast and easy access to all NCC activities. Whichever registration category selected (or whether a guest of a participating exhibitor), the badge will be mailed in advance of the conference.

For $75 (or $60, if in advance) you can register on site for the technical and professional program, conference exhibits, the Personal Computing Festival, and get your copy of the "NCC '79 Proceedings". One-day conference registration and exhibits-only registrations include corresponding Personal Computing Festival activities. Separate registrations are available for the Personal Computing Festival including the complete Festival and "Personal Computing Proceedings". Festival registrations, excluding the "Proceedings", also are available for one day or for all four days.

Conference registration in New York will begin at 4 PM on sunday, June 3, at the New York Hilton only, and will continue beginning at 7:45 AM on Monday, June 4 at the New York Hilton and Sheraton Centre (formerly the Americana) Hotels and at the New York Coliseum.

Something for everyone

Due to the large number of sessions, we listed them in our conference chart but printed technical program excerpts from those that we felt were of particular interest to you. Although we originally tried to break sessions into generic categories, the sheer number of sessions and vast coverage of so many different topics (all the way from array processing and local area networking to commercial banking automation and computer graphics in the building industries) simply made this impossible. The coverage is impressive. Chances are that if a topic is not covered in at least one of the sessions at NCC '79, then it's not worth knowing.

TECHNICAL PROGRAM EXCERPTS

Array Processing: an Innovative Approach to Scientific Computing
Session Leader: Roy D. Gwin, Floating Point Systems, Inc., Portland, OR.
Array processors are a relatively recent approach to provide cost effective scientific processing via attached processors. This panel will discuss history, philosophy, and implementation of array processors with particular emphasis on problems solving environments. Two environments will be discussed in detail. The first environment will be computer tomography which has allowed the medical profession to have a greater diagnostic capability.
The second environment will be cockpit flight simulators where advances made will allow full simulation of aircraft possible for pilot training. This panel will also discuss the basic mathematical requirements of such environments and their adaptation to array processing through the mathematical solutions of sparse matrices.

Practical Applications of Data Encryption
Session Leader: Durrell Hillis, Motorola Government Electronics Div., Scottsdale, AZ.
Two users, from different organizations in the financial world, will relate experiences in implementing data security and discuss their cost trade-off analysis leading to that implementation. an electronic surveillance expert will review the current threats associated with wiretapping and other electronic surveillance techniques. Two suppliers of standard data encryption equipment will discuss capabilities and limitations of current state-of-the-art encryption systems.

Associative Processors = Why Are They Needed? What Can We Expect in the Future?
Session Leader: Tadao Ichikawa, Hiroshima Univ., Hiroshima, Japan and King Sun Fu, Purdue Univ., West Lafayette, IN.
When we consider the rapidly developing large scale integration technology of recent years, we now need to work toward the economical implementation of application-oriented high-perform-

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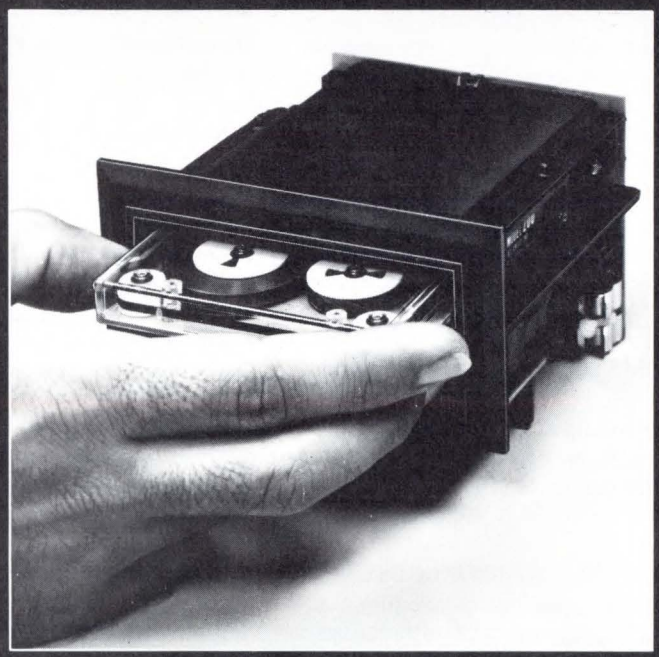

ance associative processors to meet social requirements. Session participants will discuss practical applicability of associative processors to database management and image processing problems in terms of the cost-effectiveness with theoretical and physical backgrounds of implementing the systems.

Dynamic and Reconfigurable Architectures

Session Leaders: Svetlana P. Kartashev, Univ. of Nebraska, Lincoln, NE; C.V. Ramamoorthy, Univ. of Cal., Berkeley, CA; and Steve I. Kartashev, Dynamic Computer Architecture, Inc., Lincoln, NE.

The architectures which change their structure via software to adapt to computational peculiarities of a program are called adaptable architectures. Distinguished are three classes of adaptable architectures: dynamic, reconfigurable and microprogrammable. This session makes a survey of dynamic and reconfigurable architectures. It specifies new architectural adaptations of future computer systems and outlines program analysis techniques aimed at finding these adaptations. Also considered are some specific systems equipped with dynamic and reconfigurable architectures.

Performance Modeling and Evaluation of Database Management Systems

Session Leader: Larry Kerschberg, Bell Laboratories, Holmdel, NJ.

The panel will focus on two areas of database management system (DBMS) performance evaluation: 1) design tools for logical and physical database structures and 2) modeling, measurement and simulation of DBMS. Relevant issues for design tools are their performance measures, and the incorporation of user-specifications. Parameterized modeling and validation is discussed for a set-theoretic DBMS prototype, and DBMS simulation modeling is presented as an extension to the information processing system simulator.

Data Dictionary Systems

Session Leader: Henry C. Lefkovits, Henry C. Lefkovits & Associates, Inc., Harvard, MA.

Data Dictionary Systems are receiving an increasing amount of attention and use in a large number of installations, both in database and conventional file environments. This session will focus on the various types of benefits that can be attained, ranging from operational considerations to the use of a data dictionary as an integral part of the system development process, and the concept of a data dictionary as the basis for a new information system technology.

Measurement Phases of Computer Selection

Session Leader: Sandra A. Mamrak, Ohio State Univ., Columbus, OH.

This session will address the feasibility of executing measurement phases in a comparison study of interactive services available through a computer network. Theoretical, technical and economic aspects of measuring interactive services will be discussed, both in relation to generating test workloads and doing statistically sound data collection and analysis. The emphasis will be on special problems present in the comparison of interactive (as opposed to batch) systems.

Documentation: The First Interface

Session Leader: Jef Raskin, Apple Computer, Inc., Cupertino, CA.

The first item a computer user deals with is documentation. Every user of computer equipment knows the frustration inherent in using the vast majority of manuals supplied by every computer and software vendor. This session addresses the questions: Why are manuals so often so bad? How can they be improved? Can the cost of good manuals be justified? A set of feisty speakers has been chosen to make this an especially interesting session.

Distributed System Control Architecture

Session Leader: Daniel Schutzer, Naval Electronics Systems Command, Washington, D.C.

There has been much study in recent years concerning the advantages and disadvantages of distributed processing architectures and networks. This session describes three representative applications of distributing processing. It describes some specific analyses performed in support of these particular applications. It is believed that these analyses provide general insight as to some major issues associated with the management and control of distributed processing architectures and networks.

Testing and Fault-Tolerance in Digital Systems

Session Leader: Stephen Y. H. Su, State Univ. of NY, Binghamton, NY.

Since the technology has moved into VLSI, testing becomes more important than ever. Intermittent faults are the major cause of failure. The first paper surveys the techniques for modeling, testing and reliability evaluation and fault-tolerant design of digital systems with intermittent faults. Testing schemes for computer archiecture are essentially ad hoc. The second paper identifies the likely errors in implementing an architecture and provides tests for improving the error coverage.

Simulation of Industrial Processes

Session Leader: J. Talavage, Purdue Univ., West Lafayette, IN.

Computer simulation used for the design of industrial systems will be considered from the viewpoint of two industrial practitioners and two university researchers. Application areas include discrete manufacturing systems, continuous processes and distribution systems.

Technical Aspects of Privacy Protection in Transnational Data Systems

Session Leader: Rein Turn, California State Univ., Northridge, CA.

The recent growth in international computer-communications systems has generated a new set of issues and problems. Among these are concerns of individuals over possible erosion of their privacy rights when personal data about them are sent abroad for processing and storage. Laws in several countries and proposed international agreements are responding by establishing privacy protection requirements on the operators and users of international data processing systems. This session concentrates on procedural and technical considerations that arise.

The Impact of New A/D LSI Technology on Systems

Session Leader: Rob Walker, Intel Corp., Santa Clara, CA.

A new class of semiconductor devices combining linear and complex digital functions on the same chip have recently become available — uPs with ADCs, telecommunication CODECs and filters and analog uCs. The combination of linear and complex digital circuitry on a single chip constitutes a fundamental advance in semiconductor technology, inferring both lower cost and higher performance. A variety of technologies such as bipolar processes, NMOS and CMOS are being proposed in the search for optimum price/performance.

Measurement of Software Reliability

Session Leader: T. C. Wesselkamper.

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An optional I/O processor makes it easy to add special devices. Two slots, complete with power, are ready for you to add interfaces to OCR wands, bar code readers, or whatever extra peripherals your workstation application requires.

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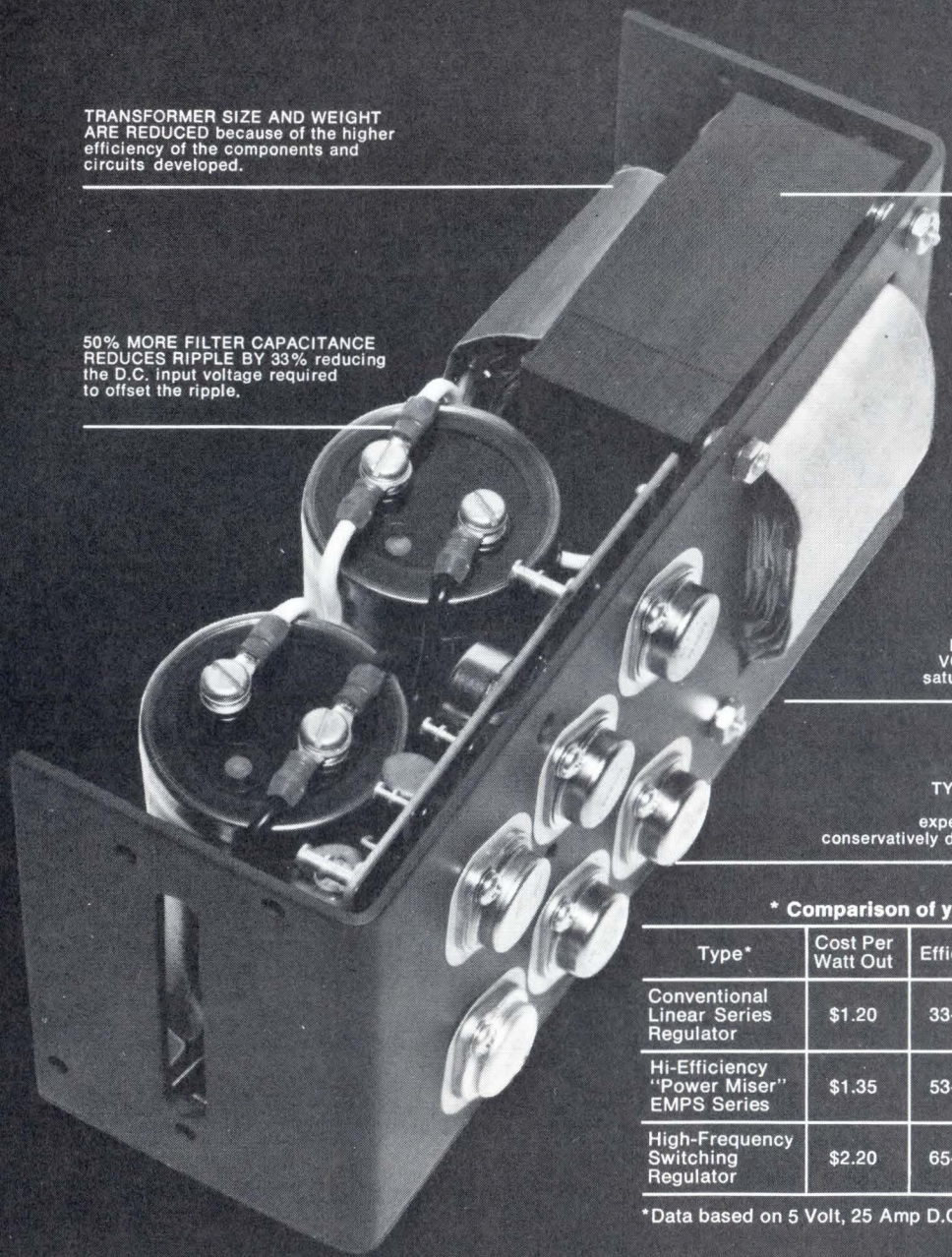

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TRANSFORMER LOSSES HAVE BEEN REDUCED 13% through the use of higher grade steel and square copper magnet wire.

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THE EMPS 5-18 (5V/18A) PICTURED IS THE SAME SIZE AS A CONVENTIONAL 5V/12A SERIES REGULATED UNIT.

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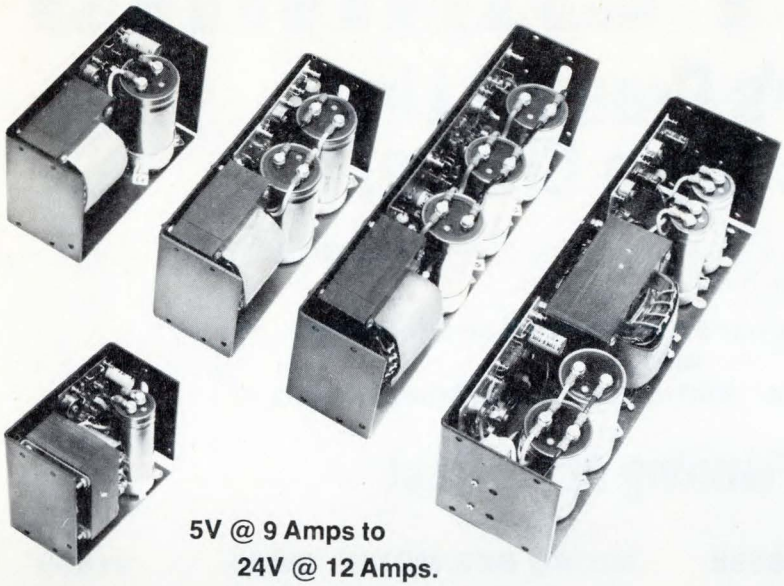
Conventional Linear Series Regulator	$1.20	33-43%	3.74 Cu. In./W.	0.27 W/Cu. In.
Hi-Efficiency "Power Miser" EMPS Series	$1.35	53-56%	1.91 Cu. In./W.	0.52 W/Cu. In.
High-Frequency Switching Regulator	$2.20	65-71%	1.34-1.62 Cu. In./W.	0.61-0.74 W/Cu. In.

*Data based on 5 Volt, 25 Amp D.C. Output Rating.

A complete series of 18 Single Output, Dual Output and Triple Output Microprocessor Models with no EMI problems...an MTBF of 60,000 to 80,000 hours...backed by a 6-year guarantee!



5V @ 9 Amps to 24V @ 12 Amps.

18 Models/ 7 Configurations

D.C. RATING	EFFICIENCY	MODEL NO.	POWER SUPPLY PRICES 1-9	10-24	25-49	50-99	100-249
Single Output Models							
5V @ 9A	54% ±2%	EMPS 5-9	99.00	94.00	90.30	87.60	85.80
5V @ 12A	54% ±2%	EMPS 5-12	109.00	103.55	99.40	96.40	94.50
5V @ 18A	54% ±2%	EMPS 5-18	135.00	127.95	122.80	119.15	116.75
5V @ 25A	54% ±2%	EMPS 5-25	180.00	171.00	164.00	159.25	156.00
5V @ 40A	54% ±2%	EMPS 5-40	220.00	209.00	200.60	194.60	190.00
12V @ 12A	59% ±1%	EMPS 12-12	170.00	161.00	154.00	149.25	146.00
12V @ 18A	59% ±1%	EMPS 12-18	210.00	199.00	190.00	184.60	180.00
15V @ 11A	65% ±1%	EMPS 15-11	170.00	161.00	154.00	149.25	146.00
15V @ 16A	65% ±1%	EMPS 15-16	210.00	199.00	190.60	184.60	180.00
24V @ 8A	68% ±1%	EMPS 24-8	170.00	161.00	154.00	149.25	146.00
24V @ 12A	68% ±1%	EMPS 24-12	210.00	199.00	190.60	184.60	180.00
Dual Output Models							
±12V @ 6A	OVER 50%	DEMPS 12-6	190.00	188.10	180.60	175.15	171.65
±15V @ 5.5A	OVER 50%	DEMPS 15-5.5	190.00	188.10	180.60	175.15	171.65
Triple Output Microprocessor Models							
5V @ 12A ±12V @ 2A	OVER 50%	TEMPS-3	185.00	175.75	168.70	163.65	160.40
5V @ 18A ±12V @ 3A	OVER 50%	TEMPS-4	230.00	218.50	209.75	203.50	199.40

*For +15V add "-2" suffix to model no.
Overvoltage protection standard on TEMPS-3 & 4, 5V. output

Specifications: All Models

A.C. Input:
5 V.D.C. OUTPUT UNITS: 105-125 Vac. 47-440Hz (derate 10% for 50Hz operation)
ALL OTHERS: 105-125/210-250 Vac, 47/440Hz

Extended A.C. Input: 100-130 Vac (derate 20%)

D.C. Outputs: See Tabulation of Models

Control: ± 5% Voltage Adjustment (Screwdriver adjust pot.)

Regulation: ± 0.05% Line or Load

Remote Sensing:
Standard on all models, (includes open sense lead protection.)

Ripple: 5mV Peak to Peak

Reserve Power:
+5% of output available for external load line drop on 5V. and 12V. units; +0.6V. on all others.

Temperature Coefficient: 0.02%/°C.

Stability:
± 0.1% for 24 hour period after 30 minute warmup

Overshoot:
No turn-on, turn-off or power failure overshoots.

Transient Response:
Output recovers to regulation band within 50 microseconds after an instantaneous load change of 50 to 100%.

Operating Temperature:
-25° to +70°C. (derate linearly above +50°C. to 40% at +70°C.; derate linearly below -5°C. to 70% at -25°C.)

Cooling:
Convection cooled for full power rating at 50°C. ambient. Forced air cooling extends full power rating to 60°C.

Protection:
Overload and short circuits: Automatic recovery foldback current limiting fully protects against overloads and short circuits. Reverse Polarity Protection: Prevents damage from reverse voltage swings. Inductive Load Protection: Prevents damage due to inductive voltage swings.

Overvoltage:
Optional crowbar overvoltage protection. (Standard on 5V. output TEMPS)

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Virginia Tech., Blacksburg, VA.
The session presents recent research results in measuring and predicting software reliability. It specifically focuses on methods which take into account the differences between hardware and software. In the two papers presented, work done in verifying the theory's validity is carefully considered. Two formal papers are followed by a discussion between their authors and two others in the field.

User Assistance In On-Line Systems
Session Leader: Richard L. Wexelblat, Sperry Univac, Blue Bell, PA.
The state-of-the-art in knowledge-based systems and in dialog processing has reached a stage where we should be able to provide truly helpful assistance to the floundering user. So far, few production systems seem to have implemented anything beyond simple Q and A. Why not systems that can converse about a problem? Systems whose response depends on the perceived level of expertness of the user?

The ANSI Reference Model for Network Protocols
Session Leader: Helen M. Wood, National Bureau of Standards, Washington, D.C.
A provisional reference model, intended to guide subsequent standardization activities, is being developed under the auspices of the American National Standards Institute (ANSI). The model currently consists of seven layers, each of which supports specific data transmission and/or data processing oriented functions, protocols, and interfaces. In this session the ANSI provisional reference model will be described and its relationship to existing and future, national and international standards will be examined.

Database Machines
Session Leader: T. H. Bonn, Sperry Research Center, Sudbury, MA.
Database machines are commanding wide-spread interest. Users are concerned over increasing database computational loads, and yet they need new functionality. A number of different approaches to database machine architecture have been reported in technical literature, there have been some product announcements, and a number of product development programs are rumored. VLSI technology is moving at a rapid pace and even some of the exotic ideas may be cost effective sooner than we think. It is time to put these trends into perspective both from the short and long term and from the user and the designer.

Languages for Computer System Simulation
Session Leader: Brian W. Unger, Univ. of Calgary, Calgary, Alberta, Canada
This session will focus on programming language facilities for the description and simulation of computer systems. The modeling of both system software and network architectures will be addressed. The work presented will include discussions of previous approaches, recent simulation languages and desirable capabilities not currently available.

Fault Tolerant and Maintainable Systems
Session Leader: Jacob A. Abraham, University of IL., Urbana, IL.
This session will focus on techniques to tolerate hardware or software failures in systems or to effectively diagnose them in order to reduce down time. Papers will be presented on a highly reliable, fault-tolerant multiprocessor for aircraft control and on a low cost, easily maintainable business computer. The question of whether the additional cost of fault-tolerance or maintainability is justified in terms of the improvement in overall throughput will be explored.

Experiences in Local Area Networking
Session Leader: Ira W. Cotton, National Bureau of Standards, Washington, D.C.
Local area data communications networks serve a limited geographic area (such as an office building or campus) for intramural data communications as well as a means of local distribution of communications from long distance data networks. This is an emerging research area in computer networking, as no local networks are available commercially on a turnkey basis. This session will provide for the exchange of experiences among those who have designed and constructed prototype local networks, with special emphasis on the problems encountered and the need for compatibility.

Benchmark Selection of Teleprocessing Systems
Session Leader: Gerald W. Findley, GSA/ADTS, Washington, DC.
The advent of plug-compatible mainframes, distributed processing, and fal-

ling hardware prices has raised new questions about the technical validity and cost-effectiveness of benchmarking during the selection of teleprocessing systems. The use of teleprocessing benchmarks, however, has been increasing. Leading CPE and benchmarking experts will discuss these developments, and other technical and managerial issues including the advantages of benchmarking, technical approaches and pitfalls, the cost for both vendors and users, benchmarking goals, remote terminal emulation and the future of benchmarking.

Microcomputers in Technical Professional Development

Session Leader: Raymond G. Fox, Learning Technology Inst., Warrenton, VA.

Continuing personnel development in the field of science and engineering is critical in maintaining technical competence in an era of rapid technological change and obsolescence. This session will look at solutions to these problems which employ the use of microcomputers in the technical professional development process. Panelists will describe methods of microcomputer uses, applications, results achieved and will identify the future potential of this technology.

Emulation Laboratories and Experience

Session Leader: Ingrid A. Eldridge, U.S. Army Communications, Research & Development Command, Fort Monmouth, NJ.

This session will describe emulation laboratories and their use by industry, government and a university. These applications include: research and development, testing and teaching. Advantages of using emulation as well as its shortcomings will be discussed. Future plans for these laboratories will also be presented.

No Patents for Software? If So, What Now?

Session Leader: John W. Behringer, Sutherland, Asbill & Brennan, Washington, D.C.

The session will review the U.S. Supreme Court's reasoning in Parker vs. Flook, holding certain computer programs unpatentable, and will look at the types of software inventions which might still be patentable, as well as alternative forms of protection, including CONTU's recommendations to Congress for modified copyright protection. The session will also examine the scope of protection afforded by confidentiality agreements and trade secrecy laws.

Computer Page Printing

Session Leader: Joel Cartun, Comvestrix Corp., New York, NY.

This session will examine the new technology of computer page printing. Current capabilities of the Honeywell PPS, the IBM 3800 and the Xerox 9700 and the experience of two user companies will be reviewed. Additional areas that will be covered include cost effectiveness, interface problems, future capabilities such as two-sided, word processing, com, graphics and color. Specialized applications including direct mail, forms, tax returns, labels, invoices and OCR will also be discussed.

Economics of Networking

Session Leader: Norman R. Nielsen, SRI International, Menlo Park, CA.

The advent of nationwide networks linking major computer facilities, the growth of distributed computing systems, and the rise of office automation has focused increasing attention upon networks, the glue that holds each of these systems together. In particular, network economics is becoming a critical consideration. Following short presentations on the papers (full text in the Proceedings), the panelists will discuss their experience with computer networking economics from both the operational and managerial points of view.

Computation Problems in Pattern Recognition and Image Processing

Session Leader: K. S. Fu, Purdue Univ., West Lafayette, IN.

This session will discuss various computation problems involved in pattern recognition and image processing applications. Special computation algorithms, computer architectures and software considerations for pattern recognition and image processing will be presented.

The Office of the Future

Session Leader: Fred Amport, Jr., A. T. Kearney, Inc., Pepper Pike, OH.

This session will describe practical guidelines for improving administrative operations effectiveness. Topics discussed include cost implications, organization strategies and alternatives, effective use of technology, governmental and competitive influences, and management's roles in effecting change. Social and economic impacts resulting from trends in technology utilization are also charted and discussed. An actual case example will be presented.

Database Evolution

Session Leader: Dennis McLeod, Univ. of Southern California, Los Angeles, CA.

The structure of a computerized database must adapt with time, as the needs and requirements of an organization change. This database evolution must accommodate changes in the user views of a database, as new information must be incorporated. Changes in database usage and performance requirements must also be handled. This panel will discuss current techniques, approaches, and research directions in addressing the problems of database evolution.

Computerized Control Systems for Automated Production Facilities

Session Leader: Leonard B. Gardner, U.S. Army Armament Research and Development Command, Dover, NJ.

Different types of control systems for automated production facilities will be discussed. These will begin with relay type logic and analog controls and progress to computers and digital controls. Included will be programmable controllers, microprocessors and minicomputers. Procedures for system design and equipment specification will be presented. The production line is treated as a continuous process and a control strategy for optimization will be discussed. Methodology used to develop functional guidelines and process control standards together with requirements for interfacing hardware and software will also be discussed.

Computer Security: Technology Vis-a-Vis Audit

Session Leader: Robert G. McKenzie, U.S. General Accounting Office, Washington, D.C.

Have the technological advances in the development of computer hardware and software exceeded the auditors' ability to adequately evaluate controls needed over information resources? This session will bring computer engineers face to face with the auditing profession to discuss the often divergent views relating to computer security technology and to the approaches that should be taken in its evaluation.

Design Issues for Word Processing Systems

Session Leader: Amy D. Wohl, Datapro Research Corp., Delran, NJ.

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This session will explore the hardware and software elements of a successful word processing system. Emphasis will be placed on the embodiment of current technology, but near-future trends will also be addressed. The session will focus on the problem of building maximum function into the system while preserving ease of training and human qualities of the machine/operator interface. Specific design issues and tradeoffs will be addressed.

More for Less with Computers in Local Government — A Challenge to Users and the Industry

Session Leader: Barry Wellar, Ministry of State for Urban Affairs, Ottawa, Canada

Thousands of local governments in North America use computer technology in conducting their affairs. After a "period of discovery," and Proposition 13 and similar initiatives, however, computer technology in local governments is being seriously challenged. Panelists address the important topic of enhanced productivity in local government through computers by discussing: status and trends of computerized applications, institutional requisites for needs-responsive computer facilities, financial information systems and fiscal responsibilities, and selecting and adapting appropriate technologies.

Advances in Secure Operating Systems Technology in DOD

Session Leader: Stephen T. Walker, Department of Defense, Washington, D.C.

The day of trusted ADP systems is at hand. After eight years of computer security research, operating systems with sufficient integrity for multilevel secure use will be available during 1979. These systems serve as existing proof to the computer industry that trusted ADP systems can be built, with profound implications on all sensitive information handling applications. Part I describes the design of three secure operating systems. This session will describe intended applications and development methodologies.

Computing in Developing Countries

Session Leader: Kasivisvanathan Vairavan, Univ. of Wisconsin, Milwaukee, WI

This session will consider some important aspects of computing in developing countries including education, training, applications, and acquisition of computing hardware. A panel discuss

sion will follow a brief presentation by each panelist.

Simulation for Predicting Computer System Performance

Session Leader: Brian W. Unger, Univ. of Calgary, Calgary, Alberta, Canada

This session will present recent work in discrete-event and hybrid simulation models for predicting the performance of computer systems.

Why Managers Fail

Session Leader: James F. Towsen, Towsen Associates, Harrisburg, PA

This practical, common sense session will zero in on the statement that MANY managers and supervisors ARE NOT regarded as assets to the organization by their peers and/or subordinates. If many managers and supervisors are not esceptionally good at the management part of their job, then NOW is the time to examine the pitfalls to be avoided. We will look at the manager who cannot COMMUNICATE and who cannot MANAGE TIME. This session will be presented in a manner that is educational, revealing and entertaining providing we can see the humor in our failures.

Software Psychology: Exploring the Human Factor

Session Leader: Ben Schneiderman, Univ. of Maryland, College Park, MD

Software psychology is the study of human performance in using computer and information systems. The techniques of experimental psychology; the content of cognitive, perceptual, social, personnel and industrial psychology, and the tools of psycholinguistics can be applied to improve our understanding of human skills and our capacity to design effective computer and information systems. Software psychology is a new "way of knowing" which complements current research and development practice while emphasizing human values. A more rigorous, psychologically based approached to systems may increase development costs and time, but long term savings result from improved system quality. Session panelists will present experimental results with an interpretation of the impact on practical and theoretical issues.

Data Processing's Proposition 13: The Software Sales Tax Issue

Session Leader: Robert M. Sherin, Nova Computing Services, Inc., Miami, FL

What we data processors are striving for is like treatment under state tax laws with those of equivalent status. The stakes are enormous: as much as one billion dollars (much more when property taxes as considered). Yet few data processor's — and even fewer lawyers — understand the advocacy. At issue is the tax treatment of data processing, not just software packages. The presentation will seek to set forth the background of old state tax law as it applies to new technology and will endeavor to show how state sales and use taxes on data processing output can be properly avoided.

EFT and Consumer Banking Automation

Session Leader: Robert V. Sabeck, Valley National Bank, Phoenix, AZ

The software and hardware technologies realistically available in the early eighties for delivery of Consumer Banking Services and then the possibilities for mid-late eighties will be presented by Mr. King. Mr. Pieper will then address the critical key elements of success — positive identification of the user (signature dynamics — voice or fingerprints, etc.) and confidentiality and security of transactions and data. Mr. Hokam will join Mr. King and Mr. Pieper in a panel discussion moderated by Mr. Sabeck.

The International Privacy Debate: Laws, Licenses and Limitations

Session Leader: Alexander D. Roth, AFIPS, Arlington, VA

Panelists will discuss foreign legislation and proposed international agreements affecting record-keeping and privacy. Emphasis will be on the impact on U.S. multinationals, with particular attention to conflicting philosophies of European and American privacy legislation and the sweeping enforcement powers of European privacy boards.

Databases in the Humanities and Social Sciences

Session Leader: Joseph Raben, Queens College, Flushing, NY

Typical of many databases in the humanities and social sciences are the inter-university consortium for political and social research and the medieval Spanish dictionary. The first, a consortium of many universities, collects and disseminates a growing base of data derived from census reports, public opinion polls, and similar materials. The second, oriented toward the publication of a dictionary, is also a computer-accessible archive of the Spanish language in its formative years.

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People Power — The Key to Effective Management of Data Processing Projects

Session Leader: Loretta A. Pitchell, Burroughs Corp., Atlanta, GA

The success or failure of any data processing project is dependent upon people. Management of data processing projects is not unique. Managers must get control of the timing and content of what they do. This involves developing a strategy to manage your boss, your peers, and your subordinates. To properly manage requires discretionary time. The profession manager eliminates subordinate-imposed time giving him more time for planning, organizing, leading and controlling. This session will attempt to demonstrate how to perform project management leadership effectively and how to handle different personality types and accomplish goals in a timely, effective manner.

Issues and Policy Concerns in Health Computing

Session Leader: Ruann E. Pengov, Office of Technology Assessment, Washington, DC

Two representatives of the executive branch and two representatives of the legislative branch will form a panel to address the current implementation of federal policy and current legislative activity related to health computing.

Trust and Securities Industry Automation

Session Leader: Junius W. Peake, Securities Industry Consultant, Englewood, NJ

Messrs. Chapdelaine, Korins and Popper will discuss and illustrate examples of working real-time systems applications in use in the investment and banking community. These include a new trading support system for municipal and government securities used by hundreds of dealers; a stock trading system which may well be a prototype for future markets, domestic and international; and a recently-developed trust, portfolio, record-keeping system.

Computer Communications and the International Data Marketplace

Session Leader: L. Dan O'Neil, National Telecommunications & Information Adm., Washington, DC

A status report of international negotiations relating to communications facilities, planning and ownership. DD

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TROUBLESHOOTING MICROCOMPUTER SYSTEMS

With Smart Multimeters

Ed Donn and Bill Rochat
Electro Scientific Industries
Portland, Oregon

Microcomputers are creating a mammoth troubleshooting problem. Even a simple failure can create bizarre symptoms. The technician's old friend, symptomatic troubleshooting, won't work; besides, we are running out of technicians who can do high level troubleshooting, and we can hardly afford the time to do it ourselves. The answer is better tools using modern microprocessor technology in innovative ways. The answer is also fresh new approaches to troubleshooting made possible by the new tools.

Many of the most time-consuming, baffling system probelms are really simple circuit problems that nobody has found a simple solution to yet. Over 75% of the faults that occur in microcomputer design and production are still simple faults like opens and shorts. And, when μC products get into the field, their maintenance technicians can spend more time troubleshooting bad power mains than bad LSI. Tools for these boring, laborious problems have been slow to improve. Logic state analyzers, μP development systems, and some production test systems cannot locate the shorts, opens and power problems that take much of our troubleshooting time.

Modern μP technology can transform a simple multimeter into a powerful troubleshooting instrument. With it you can find the actual location of shorts on busses, stuck-together gates, bad power distribution and grounds, and drooping power mains. It can also do simple things simply, like holding a reading until you are finished with it, and measuring current without getting into the circuit or going through a gyration of probe and range changes. It can do exotic measurements, like digital averaging, data logging, measuring to a preset tolerance, and storing and processing measurement results.

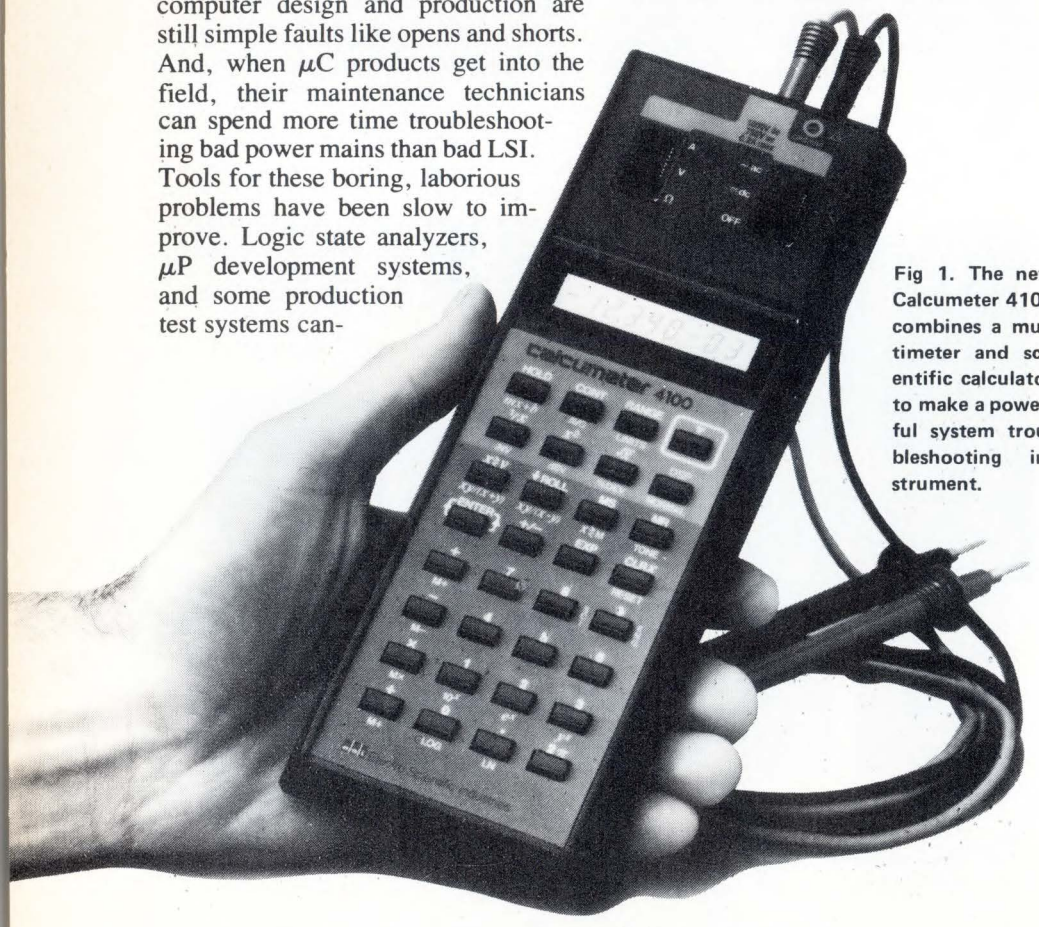

Fig 1. The new Calcumeter 4100 combines a multimeter and scientific calculator to make a powerful system troubleshooting instrument.

So what do you do with a handheld meter that is as powerful as some instrument systems of a few years back?

Throughout the μP saga we have gotten through the toy-to-tool phase of calculators, programmable calculators, and microcomputers by sharing our applications. Such sharing opens our imagination to areas where we have done without good tools for so long we have stopped thinking about them. Following are three such applications in important system-measurement areas: debugging logic, checking grounding and power distribution, and long term monitoring.

Troubleshooting logic

Engineers love inventing and hate troubleshooting. The Calcumeter 4100 (**Fig 1**) is a useful troubleshooting tool, as significant as the logic probe and logic state analyzer. It can be used as a universal static logic probe. It has a LIMITS mode that displays a floating bar, like an analog meter, but between precise limits. Set the limits to the power voltages, and you have a universal logic probe that is good for TTL, all varieties of MOS and even ECL. This mode gets users through any static logic errors in a newdesign and paves the way to solve interconnection errors.

Systems engineers think about systems, and don't like to think about interconnections — so their interconnections often don't work! For many of us, interconnection errors outnumber all our system, logic and timing errors. When our designs don't work, it's usually because we or a solder splash has wired something to a wrong pin.

The best indication of a wiring error is an illegal level. Logic probes warn of this problem, but you still have to resolve it manually and visually. The Calcumeter takes a few crucial steps closer to the solution. First you can measure short-circuit current at the flick of a switch (no probe and range

changing is required). If the current is a few mA from pullup resistors, then the problem is a floating input — a wire is missing. But, if the current is tens of mA from a loaded down gate somewhere, then the problem is an accidental Wire-Or of two outputs — a wire is shorted. Knowing which problem you are looking for saves a lot of manual troubleshooting.

Signal wires not only get accidentally tied to each other, they also get tied to ground and Vcc. You can spot this common problem automatically in TTL and ECL designs. Simply set the limits just inside the power supply levels; 0.05 and 4.8V for TTL and −0.4 and −4V for ECL. Now if the level is from a power rail instead of a logic gate, you can get an instant beep and error message from the Calcumeter. You can immediately see, with each touch of the probe, shorts to power rails, shorts between gates, floating opens, and legitimate 1's and 0's.

A simple feature that allows the last trick to work and saves a lot of strain, in general, is a footswitch on the Calcumeter. Every instrument should have a footswitch so you can tell it when to measure and hold. Without it the Calcumeter would beep a meaningless warning when the probe was lifted in the last setup. With it you just probe, tap the footswitch, then turn around and see what happened. No more arm and eyeball gymnastics to take a measurement.

Sometimes during logic probing, you want to know the exact voltage you have measured instead of 1's and 0's. Just push DSP and the bar display will be replaced by a conventional voltage reading. On the next measurement it will go back to the "logic probe" format. Of course, if you want it permanently changed to a conventional display, just push SHIFT/NORMAL and your "logic probe" will turn into a digital voltmeter again.

Shorts tracing

The only thing harder to find than active shorts on a live board are active shorts on a three-state bus. Three state busses can be checked easily with the flick-of-a-switch ammeter. This simple measurement will quickly tell you, before you get any further, if the bus is being loaded by active devices or too much fan-out. Later on bad busses will cause exasperating symptoms. Then the microprocessor will crash and you will go through a lot of thrashing trying to isolate the problem in the data domain with a development system or

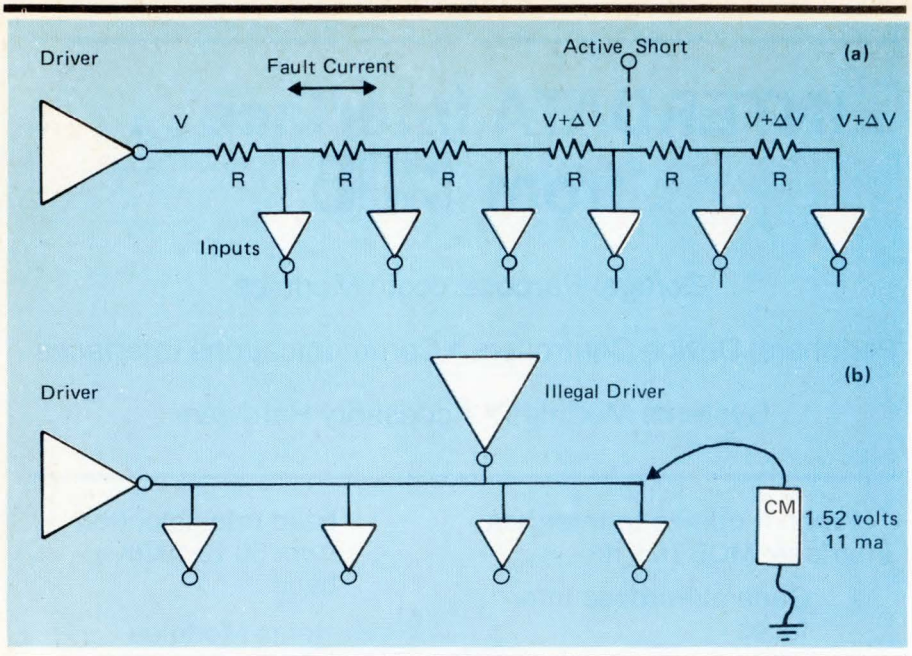

Fig 2 (a) Schematic of an active short. In this application the calcumeter works better than a 4 terminal milliohmeter, because it works on a live board.
(b) An illegal level, 1.52 volts, is a clue to a fault, but is it an open or an illegal driver? Short circuit current tells which.

logic analyzer.

Calcumeter-type instruments easily find shorts to active devices. In this application, it is used as a high common-mode rejection microvoltmeter with measurement memory and processing.

Fig 2a shows the schematic of an active short. The driver is tied to several inputs and a short. The short causes a fault current to flow through the printed circuit trace. Upstream from the short the voltage will gradually rise or fall on the way back to the driver. Downstream, however, the voltage will remain nearly constant (some pulldown current can flow, but it will be much less than the fault current).

Finding the short is easy with the Calcumeter. First, use it as an ammeter to see if the driver can supply current. If it can't the driver is bad or the trace is open back to the driver.

If plenty of driver current is flowing, then follow the voltage drops from the driver to all the inputs along the fanout by placing the black lead on the driver and the red lead on each input. Use the footswitch to easily record the measurement. Store each measurement in the calculator's stack by pushing ENTER each time. When you get to a point where the measurement doesn't change, you have found the short. The stack gives you plenty of history to go by without having to write anything down.

The voltage drops are going to vary with fault current, lead length, and trace width. Trace resistance will vary from about 10 to 40 milliohms/inch as the width varies from medium (1.5 mm) to fine (0.5 mm). A 10 mA fault current will produce 100 to 400 μV/inch and give a resolution ranging from 0.1 to 0.025'.

You can get more fault current and resolution by clipping an incandescent lamp from the driver pin to the appropriate power rail; now you will get hefty fault currents even for MOS circuits.

You can refine the measurement further with four keystrokes. ENTER the first measurement at the driver. On subsequent measurements, store each new measurement, subtract, recall and enter. Now the unit will display and store voltage differences between each node; you will have the last three nodes of history without ever having to write anything down or move more than one probe.

With six keystrokes, the instrument will measure the voltage drop per inch between each node. Here is the measurement sequence:

HOLD	Take 1st measurement
ENTER	Enter the first measurement
HOLD	Move probe down trace Take a new measurement
MS	Temporarily store it
−	Subtract from the last measurement
(key in length)	Estimate the trace length
÷	Divide to get volts/inch
MR	Recall measurement

Want even more refinement? If the signal-to-noise ratio (SNR) is bad, you can digitally average as long as you want to obtain better resolution and accuracy. If storage of past measurements is important, you can attach a miniature printer and print out everything you measure.

Continuity

When I have miswired a cable, I use the "calibrated-circuit buzzer" mode of the Calcumeter. Set the lower range to −1 ohms to get it out of the way and the upper range to 100 ohms. Now the meter will beep if it finds an open greater than 100 ohms. If you prefer beeping on continuity instead of open, then set the lower threshold to 100 ohms and the upper threshold to 20K. Tie a 10K resistor across the leads to fool the meter. Now it will beep if the resistance is less than 100 ohms.

Power and ground distribution

Another simple circuit problem that can mascarade as a complex system problem is power and ground distribution. I usually ignore the mind-dulling task of methodically checking grounds, power, and interconnections. I sometimes sharpen my wits by troubleshooting a mixture of system and circuit problems all at once in the data domain. But, don't do that. The Calcumeter makes power and ground distribution testing almost fun. If these problems are not solved early, beore you even turn on the clocks, they can easily become production nightmares. If they get into the field, they will cause the worst of all faults — intermittent faults.

Before you even turn on the scope, step back to DC and make sure all the ohms-law stuff is solid. Excessive voltage drops and ground impedance are a sure precursor of both circuit noise and erratic systems. Ground losses eat into your noise margins, induce common mode noise, and reduce the voltage across the ICs (which reduces noise margins further). LSI has less tolerance of V_{cc} errors than standard logic (±5% instead of the usual ±10%). Vary the V_{cc} voltage to a microcomputer sometime and notice the bizarre failure modes. You could troubleshoot one of them for hours without realizing it was just a bad power supply voltage.

First check out your grounds by clipping the black lead to the "system ground," hopefully a fat bus bar connecting the edge connector grounds. Set the upper limit as tight as you can afford, say 0.2V, and the lower limit to −0.1V. If the upper limit goes off,

ground resistance is too high. If the lower limit goes off, you aren't really on ground and you need to either subtract the negative reading from the others (use Mx+B mode) or change grounds.

V_{cc} can be tested on each board by setting the limits to 4.75 and 5.25 or whatever is appropriate. Or, you can enter the nominal voltage, 5.00 and measure percentage deviation directly on the meter. Include the effects of ground shift by either subtracting it from the V_{cc} reading (use the Mx+B mode) or putting the meter ground on the same IC where you are measuring V_{cc}.

Circuit measurement

The Calcumeter makes it easy to find the current in bias networks and active devices. Key in the load resistance, take the reciprocal and store it. Store 0 in the Y register. Change to Voltage, Mx+B, and connect the meter to the load. The meter will now read DC current directly in engineering units without having to clip into the circuit.

To measure power in the device, ENTER the current reading, go to NORMAL mode, measure voltage, subtract from V_{cc}, multiply, and you have power directly in engineering units.

Long term monitoring

As μC-based circuitry expands into the industrial world, a common source of field failures will be power mains. The microcomputer will often be sharing a power main with a refrigerator compressor and cashier's space heater; in these applications, line voltage variations can be an early warning of problems to come.

The Calcumeter and its companion printer make an inexpensive and very accurate data logger for such applications. The printer has a timer than can initiate a measure-and-print cycle from once every 3/s. to every 3 hrs. The Calcumeter, instead of doing nothing, can average the line voltage between recordings. It can average over intervals ranging from 1/0.5 sec. to hours or even days, if you like. Other innovative troubleshooting instruments are now coming on the market, and there is no excuse for the microcomputer system designer not to take advantage of them.

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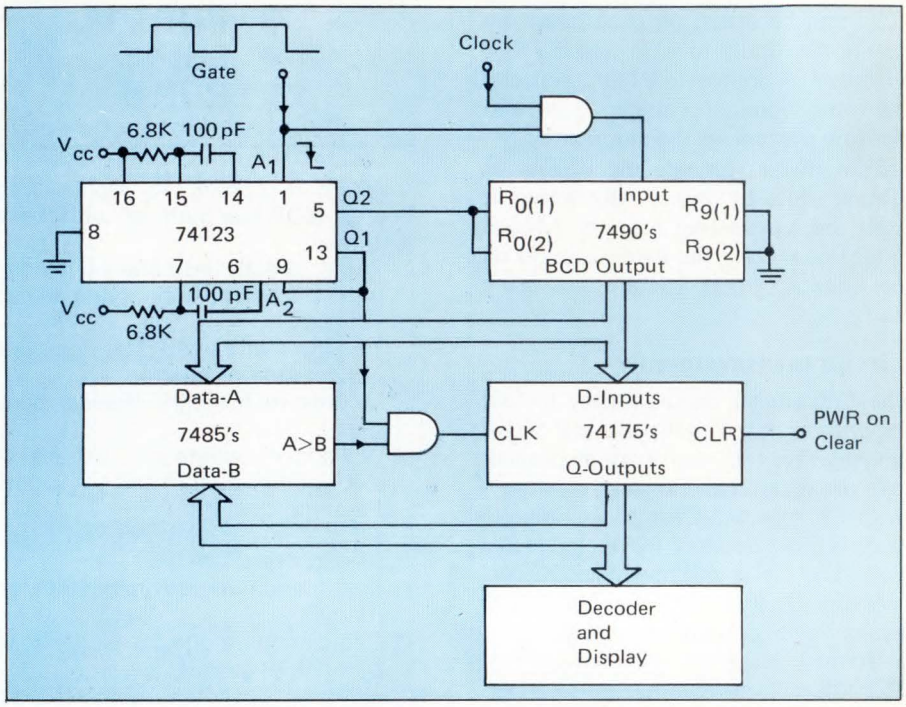
DESIGNERS' NOTEBOOK

A Simple Digital Peak Detector Circuit

Some applications involve the counting of peak value of the count. Many conventional circuits involve too much of the hardware to implement decision making circuits and also require the separate storage for storing the digital information.

The circuit shown uses counter storage itself. The decision making circuit consists of comparator (cascaded 7485s) and an AND gate. The A > B output of the comparator is AND gated with monostable output. The monostable gets triggered at the trailing edge of the gate waveform. So that decision is taken after the counting is over. The incoming count (data A) is compared with the previous peak count (data B). After the comparison, the counter data is transferred to the latches (74175s) only when incoming count is greater than the previous count.

With slight modifications, the circuit can be very easily converted into peak detector for slowly varying hydraulic waves. In such applications data is supplied from A/D converter instead of supplying it from the counting circuit. The STATUS terminal is used to trigger the monostable which confirms the completion of analog to digital conversion. This circuit does not suffer from the drift having a unique advantage over the analog peak detector circuits.



This digital peak detector circuit boasts simplicy and circumvents drift problems of analog peak detector circuits.

CEERI Colony, Qt. G-91, PILANI (Rajasthan) 333 031, India.

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Four-Quadrant Analog Divider

Analog division is frequently performed by the circuit shown in Fig 1 using a 4-quadrant multiplier and an op-amp. The circuit obeys the equation:

$W/R_1 - XY/R_2 = 0$. Hence:

$$Y = (R_2 W)/(R_1 W).$$

However this arrangement becomes unstable for negative values of the input X due to positive feedback around the amplifier. The problem is overcome by the circuit of Fig 2, which obeys the equation:

$$XW/R_1 - X^2 Y/R_2 = 0$$

The polarity of the term X^2Y is independent of the polarity of X, and so the feedback is stable for all values of X. The circuit is a true 4-quadrant divider.

J.R. Ball, 7 Moorfield Rd., Woodbridge, Suffolk, Eng.

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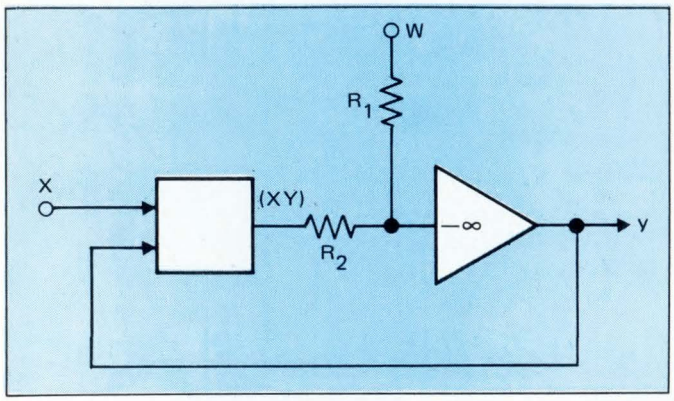

Fig 1 Traditional analog divider uses 4-9 quadrature divider and op amp, with feedback configuration shown here.

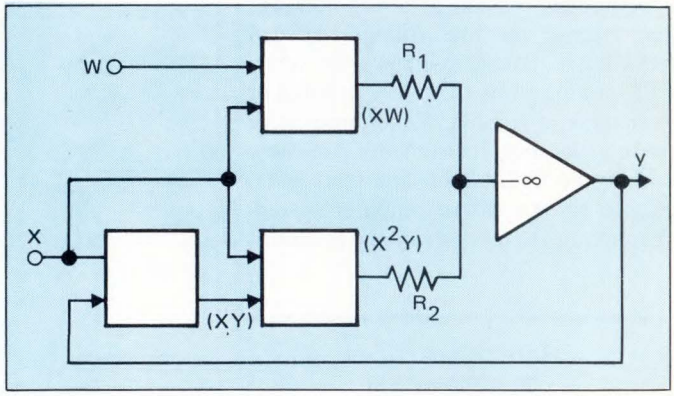

Fig 2 For x<0, positive feedback creates an unstable circuit.

Multiprogramming with uPs

A well-known method of increasing the total memory span of a microprocessor is to use a multibit addressable latch (which holds the most significant end of the memory address) accessed by the micro as an I/O port. For those micros (e.g. 6800 and 6500) which do not provide any separate I/O instruction, expansion of memory size in multiples of 64K bytes is not possible in this way. The circuit described here overcomes this and other practical difficulties. At the same time, it provides a very desirable feature for such a large system. This feature enables the user-programs to be relocatable, effectively providing a multiprogramming environment as in the "minis" and the "mainframes."

The present circuit produces a total of 20 lines for the address bus (A'_0–A'_{19}), of which the least significant 12 lines (A'_0–A'_{11}) are taken directly from the microprocessor. The total addressable memory area (1024K bytes altogether) is logically divided into 256 pages of 4K bytes each. The heart of the circuit is an 8-bit register and an 8-bit adder. The register (two 'LS175 ICs) is used to hold the base address of the "currently running" program (in units of 4K bytes). This base register and all other peripheral control registers including I/O latches should be located in the top page (i.e. A'_{12}–A'_{15} all high) of the microprocessor's own address field. An active low signal SPS (system page select) is provided for this purpose. The base register itself should be selected by using the input BRS (base register select – active high) depending on its position in the page.

Each "relocatable" program may be allocated only one page of memory space or as many as 15 pages. Internally each program assumes an address field from 0000 hex to the "allocated" maximum. Externally the base address of the program is added to the output address from the micro to produce the composite address A'_0–A'_{19}. Two 4-bit adders ('LS283) are used for this purpose.

The exception to this rule is that when the microprocessor addresses the system page the contents of the base register is not added to the micro's output address and A'_{16}–A'_{19} are forced low. Eight 2-input NOR gates force the outputs from the base register low when the system page is addressed. Thus it is ensured that each

program can address any I/O register located in the system page (defined in this context as A'_{16}–A'_{19} all low and A'_{12}–A'_{15} all high) and also call a system subroutine located in that page without reloading the base register. Since the vector addresses for interrupt, non-maskable interrrupt and software interrrupt of a 6800 microprocessor are located in the system page, the micro has to access this page any time irrespective of the contents of the base register.

The delay introduced by the adder to produce a stable address in an R/W cycle is 40 nsec max. A compromise solution is provided by delaying the system ϕ_2 for about 24 nsec (by using 4 'LS04 inverters) so that standard peripheral adaptors can fit well in this system.

The reset signal to the microprocessor may also be used to reset the base register as shown in the circuit diagram. Finally, the outputs from this circuit, namely, ϕ_2 and A'_{12}–A'_{19}, have to be buffered for further use.

De Zain ul Abedin, Plessey Telecommunications Ltd.

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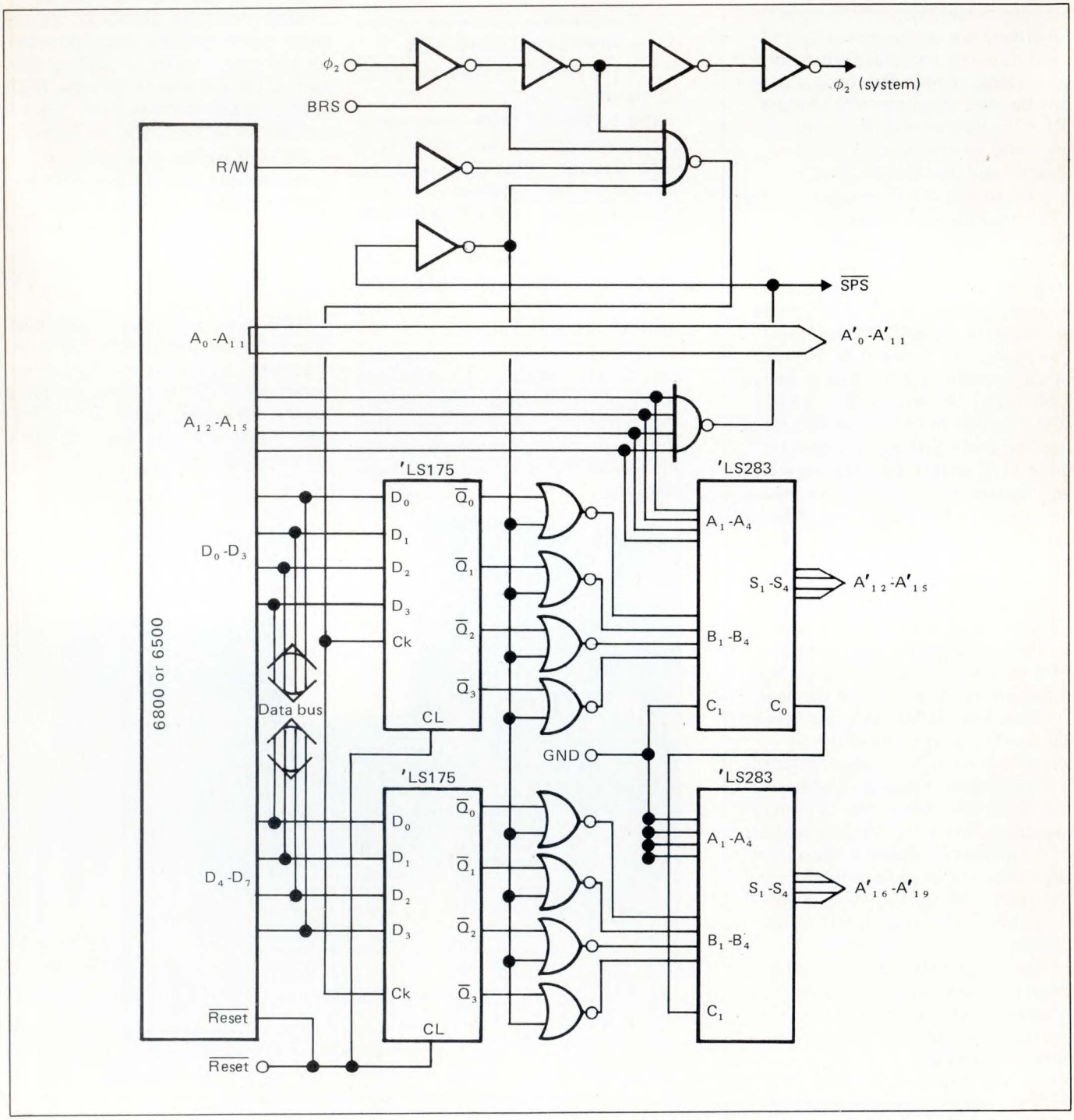

This multiprogramming permits memory expansion and anables user programs to be relocatable for the 6800 and 6500-type μPs. The 'LS 175's are positive-edge-triggered D-type flip-flops; the 'LS 283s, 4-bit binary full adders with fast carry.

16-Channel Bar Graph Video Display

Bar graph displays offer some advantages over numerical indications, especially when a large number of parameters have to be observed.

In control rooms, the operator can determine at a glance the relative value of each displayed variable. The following article describes a circuit that permits display of 16 bar graphs with a 0.4% resolution on a TV video monitor (50Hz), an instrument that is normally available in control rooms.

The circuit shows 2 counter sections, the horizontal counter and the vertical counter.

The horizontal counter is driven by a 10MHz clock and divides the screen horizontally in 16 equal slices (counter outputs H64, H128, H256 and H512). Counter output H32 provides spacing between bars.

Additional decoding produces the HSYN and HBLANK signals (15.625KHz).

The vertical counter is clocked by the HSYN pulses and divides the screen vertically in 256 lines, represented by vertical outputs V2 through V256 (8 bits).

These outputs are connected to the digital inputs of an 8-bit DAC. Current output of the DAC is converted to a positive 10V/256 steps staircase signal with a 741 OP AMP. The second 741 inverts the staircase and drives one input of the 311 comparator. The other comparator input is connected to the output of a 16-channel Analog Multiplexer 506 (MUX).

The MUX address lines are driven by the 4-counter output H64 through H512. So, during each horizontal scan, the 16 analog inputs (0 + 10V) are connected sequentially to the comparator input and compared with the inverted staircase signal (corresponding to the vertical position of the spot on the screen). The comparator output represents the video information (0 = Blank, 1 = Dot) and is OR'ed with the hor. and vert. blanking signals.

VSYN (50Hz) and HSYN are also OR'ed and both OR outputs drive the output transistor, which sends a 3-level composite video signal to the TV video monitor. A grid pattern, decoded from 4 vertical counter ouputs, is super-imposed on the screen and gives 16 equally spaced horizontal grid lines.

With an additional Multiplexer, the number of input channels can be doubled (32). However, Mux. address and

Space decoding should then be changed accordingly.

R. Romyn, CERN/EF Div., Geneva, Switzerland.

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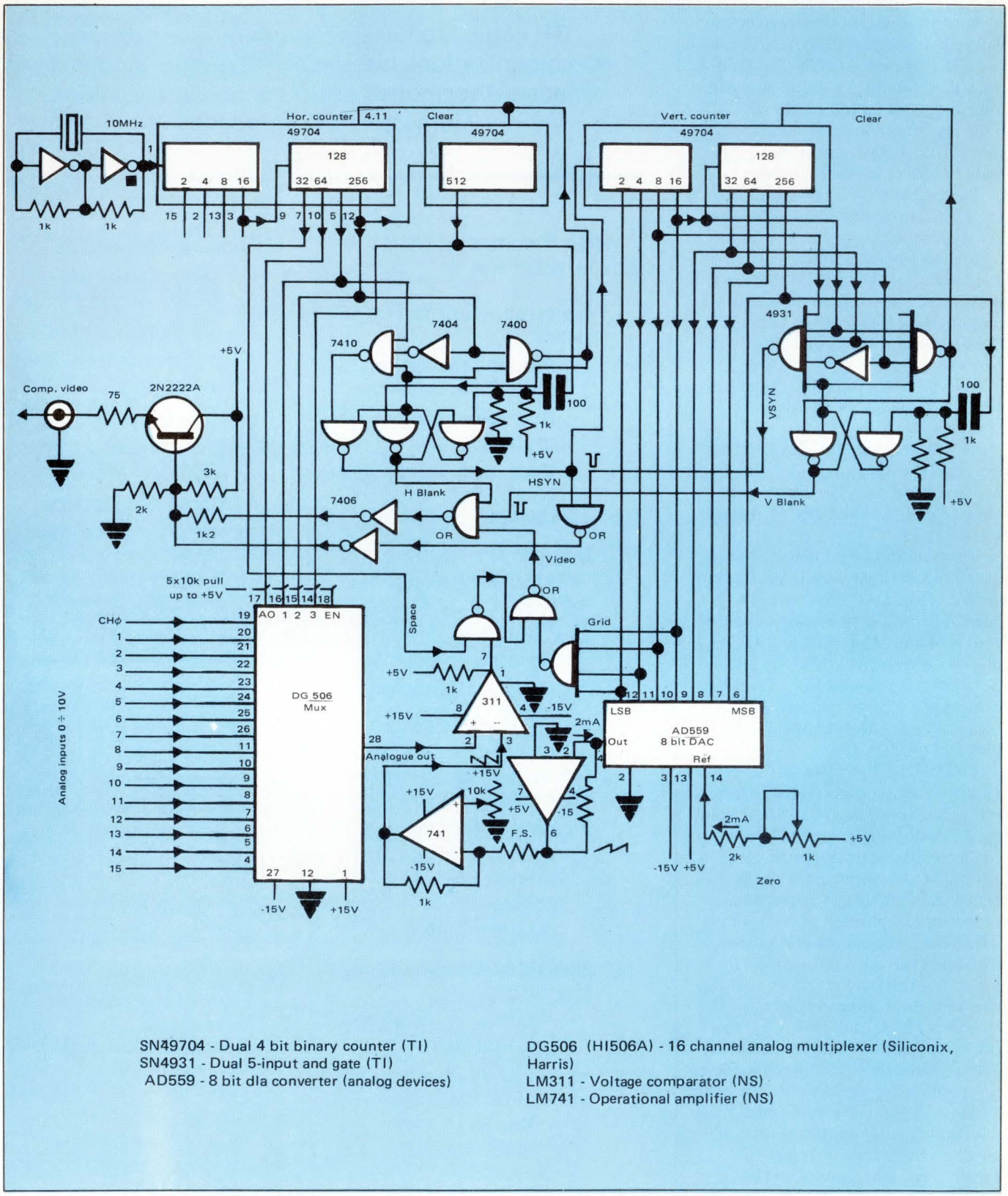

SN49704 - Dual 4 bit binary counter (TI)
SN4931 - Dual 5-input and gate (TI)
AD559 - 8 bit dla converter (analog devices)

DG506 (HI506A) - 16 channel analog multiplexer (Siliconix, Harris)
LM311 - Voltage comparator (NS)
LM741 - Operational amplifier (NS)

This bar graph video display circuit generates 16 vertical bars on a TV monitor. To double the number of input channels, add a multiplexer and change MUX address and space decoding.

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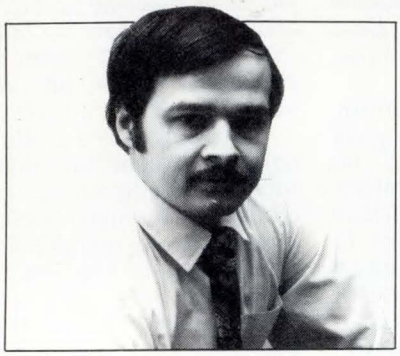
SPEAKOUT

Paul Snigier, *Editor*

Riding the Crest of Growth



A cataclysmic tidal wave of sudden change is sweeping through the electronics world and nothing will be the same again. The electronics trade press is also riding this crest of growth and sudden change, with the accelerating pace of electronic developments forcing the electronics trade press to continually reevaluate its coverage. Like everyone, our editors at Digital Design continually seek better ways to present new ideas. Over the past year, we introduced several ideas in a manner most useful to you. We produced a special issue in September on one subject (printers) and a special December Review/Preview issue. Both received numerous favorable comments from our readers. Further, we published Designer's Notebook ideas, not to mention several staff written-reports. We did this and more, yet still provided a balanced mixture of articles covering μPs/μCs, systems design, instrumentation (and even interconnects and packaging), printers, CRT terminals, data acquistion and other high-interest systems design articles of interest to "the systems integrator."

But now we anticipate expanding the depth of our coverage. Because the electronics industry is changing so rapidly, Digital Design's editorial plan is subject to change as necessary to cover these new developments. What's in store? That's where you come in. We'd very much like your evaluation of our past efforts and what you want to see in upcoming issues of Digital Design. If you could do us a favor, please take a few minutes to circle the numbers on the front of a Reader Inquiry Card and mail it to us. If you don't see your preference listed on this page (or you don't like some things we cover), then we still want to see your comments; simply write them on the line provided under "Comments" on the Reader Inquiry Card. We appreciate your help on this. We read all RIC comments and we will give your inputs careful consideration in our planning.

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MICROCOMPUTER SOFTWARE
Lowers Parts Count

Larry A. Solomon and Dennis Block
RCA Solid State Div.

Advantages of choosing a microprocessor-based system over designing with standard ICs are well known. One of the principal reasons is reducing parts count. All but the very simplest systems consist of several ICs — RAM, ROM and I/O devices. A major design consideration involves tradeoffs between hardware and software, which reflects itself in the ROM to I/O mixture. The economics indicate that the more functions handled in software, the less expensive and more flexible the system will be. Thus, the best departure point for a design is to try to do everything in software; then, functions are relegated to hardware as the speed/processing capability of the CPU becomes taxed. Here are several examples that illustrate the approaches for handling typical I/O functions by means of software.

A classical system

Consider the simple system diagrammed in **Fig 1** — a simple input device, microprocessor and output device. The specific functions have been purposely omitted. A classical software control flowchart for such a system is shown in **Fig 2.** We see the standard initialization procedure followed by an input, processing and output procedures, and a final loop back to repeat the action again. Without knowing the details of the hardware or software design nor the specific application in mind, certain predictions can be made about this system.

The software cycle time will affect the type of input and output devices chosen. First, let's consider the software cycle time, the time to go completely through one loop of the procedure. The cycle time is the sum of the time spent in each portion of the software, including input, processing, and output. Since the program apparently waits for an input, the time spent in the input block is indeterminate. Thus the system cycle time is indeterminate. This has immediate impact on the selection of both input and output devices used in the system. The output device, for instance, must be capable of operating for prolonged periods without processor attention. Therefore, it must be a device that is self-refreshing or contains a latch. It certainly cannot be dynamic, since the simple software structure shown thus far has no provision for refreshing. As dynamically refreshed displays have the potential for lower cost, we should consider the static requirement as a serious drawback to the straightforward, simplistic approach. Next, consider the input device. Perhaps it presents data to the processor at an uneven rate, which is most certainly true if the entry device is human-operated. If a keyboard is being serviced, for example, the time between keystrokes can vary from a few milliseconds to several seconds or minutes. Yet, the processor must be fast enough to respond to the fastest keystroke rate. If each keystroke results

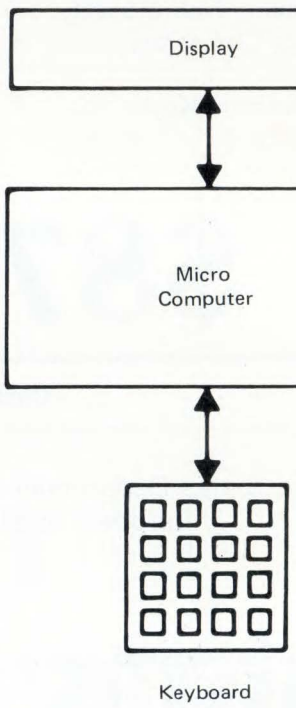


Fig. 1 Starting point. This classical system can be implemented in varying combinations of hardware and software.

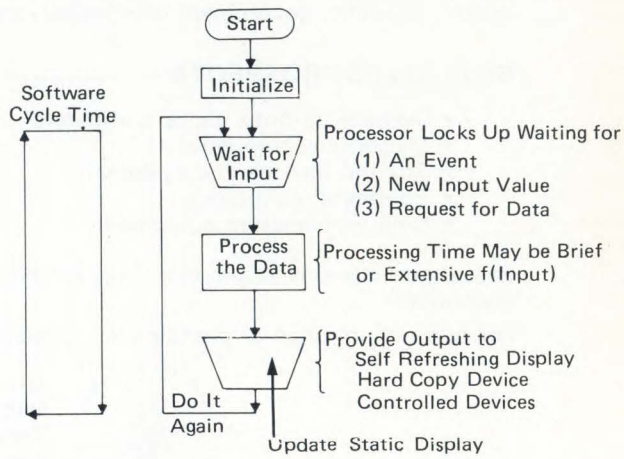


Fig. 2 Software cycle for our generalized system can be divided into three parts — input, processing and output.

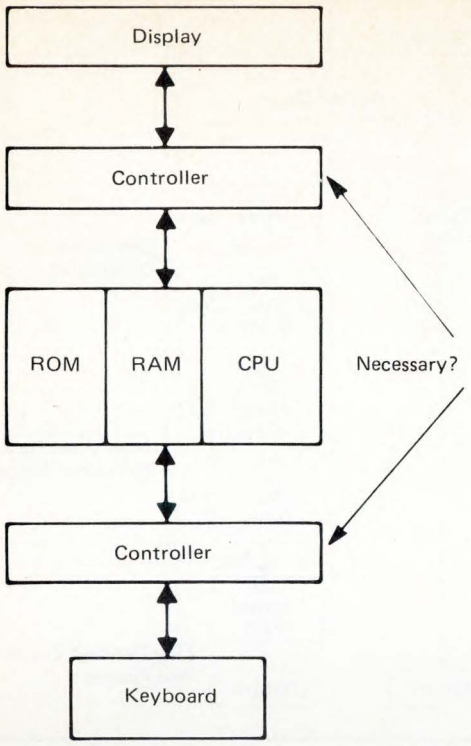


Fig. 3 System defined in small blocks Ideads to the questions "How much of this hardware is necessary?" ROM, RAM and CPU are essential, but controllers might be replaced by software.

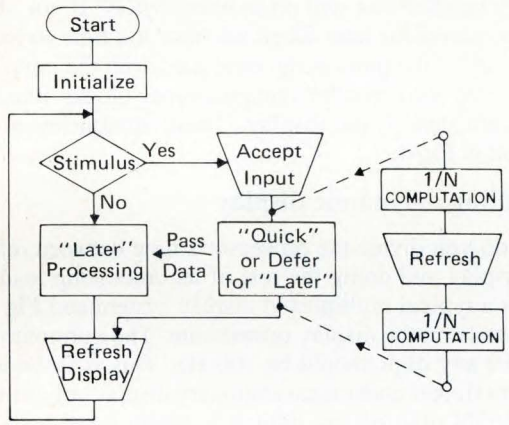


Fig. 4 Balancing the load with software. System decides whether to accept input, do computation or refresh display.

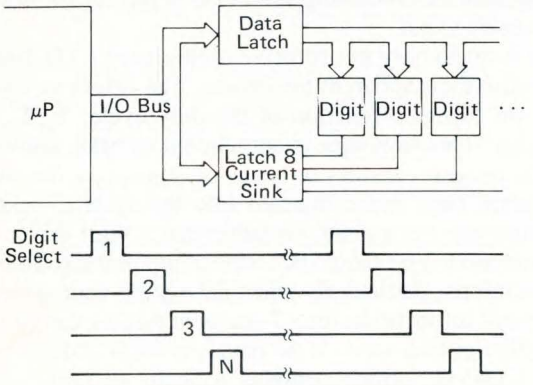


Fig. 5 Typical multiplexed display system.

in some serious analysis on the part of the microprocessor, the minimum time between keystrokes might have to be lengthened. If the microprocessor must additionally activate some hard-copy device such as a drum printer, several hundred milliseconds might have to be dedicated to the output processing block as well. In that case, we might be designing the system rather than the reverse. To compensate for lack of time between keystrokes might have to be lengthened. If the microprocessor must additionally activate some hard-copy device such as a drum printer, several hundred milliseconds might have to be dedicated to the output processing block as well. In that case, we might be designing the system rather than the reverse. To compensate for lack of time between keystrokes, you could choose a microprocessor that can "handle the job", i.e., one that goes faster (but costs more). Another solution to the time problem could be to design in an "intelligent" keyboard controller or some sort of buffering device to smooth out the input rate. However, resorting to this additional hardware may not be necessary.

There is a third case in which the simple structured system doesn't work at all. If, for instance, the input to the system was a requirement for some lengthy output report, then while the system was busily processing the request, no new input could be presented. Any input during that time would be lost.

System performance can be limited by either hardware or software. We now see that the system "specified" in **Fig 2** is a "simple" one, but one with severe limitations and pitfalls. The system will inherently go from an I/O-bound block to a processing-bound block and back to being I/O-bound. Also, since it makes no attempt to level peak loads, this system will waste the microprocessor's power. We will next examine how to minimize wasted processing time and level loads to a manageable degree.

Hardware-software tradeoffs

The microprocessor system has to have ROM, RAM and CPU. By using them to a greater capacity, other hardware can be eliminated.

Let's take a closer look at the proposed system and see what is involved in the hardware. **Fig 3** has broken down the initial diagram into smaller blocks. The display now has some controlling circuitry, as does the keyboard. These are shown along with the indispensable elements of any microprocessor system — ROM, RAM and CPU. The system must have these, but must it have the controllers? Can we perform the controller function by marginally increasing the cost of some other portion of the system? Perhaps!

The software approach distributes the workload. By doing these functions in software, we may eliminate the controllers at the cost of enlarging the system ROM. But, here's an interesting fact in IC economics. Since ROMs come in fixed increments, it is often no more expensive to have a program that is 1024 bytes long than one that is 527 bytes, even though one is almost twice as long as the other. To take the software approach, we will restructure the simple-minded solution originally suggested and, through workload distribution and continuous processing, obtain minimum system hardware. We will change our approach so that instead of waiting for an input to take place, we will simply look at the input periodically. If no input is present at that time, we will skip the input operation and go on to see if something else remains to be done. Refreshing a dynamic display, for instance, always needs to be done, and so a dynamic display meshes neatly with our revised concept. After refresh, we will again look for an input. If one should now be pending, it will be accepted. Now we must make a decision. If the input can be

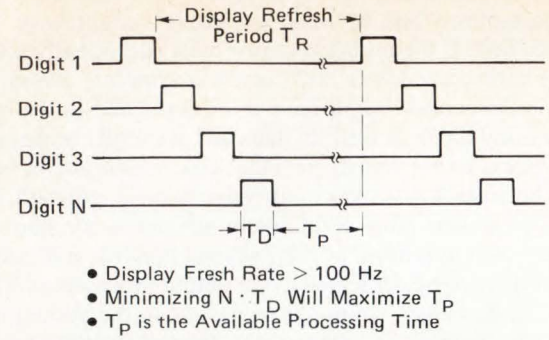


Fig. 6 Display refresh rate affects both software and hardware. Refresh rate must be fast enough to prevent flicker, but still allow time for processor to do other work.

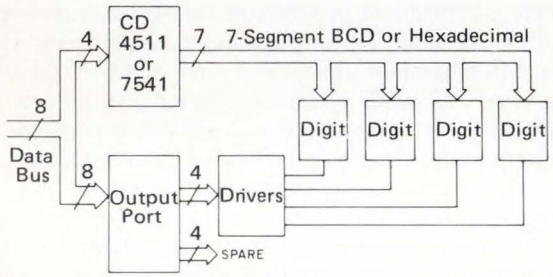


Fig. 7 Display information handled by hardware using MSI devices.

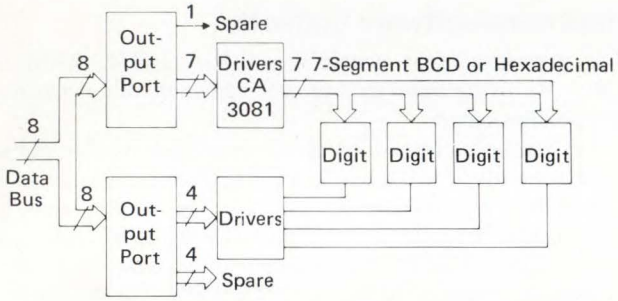


Fig. 8 Same display as Fig. 7, but handled by an output port and software look-up table.

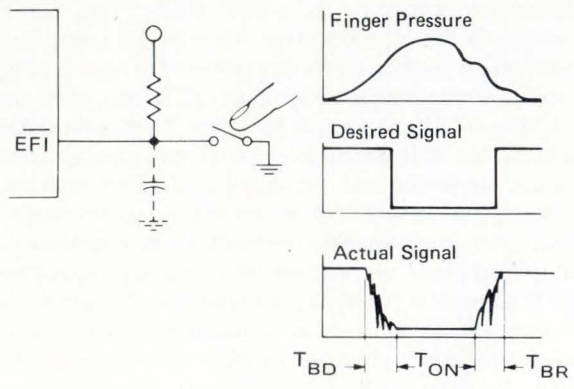


Fig. 9 Switch inputs present a problem because of switch bounce, which can be solved via hardware or software techniques.

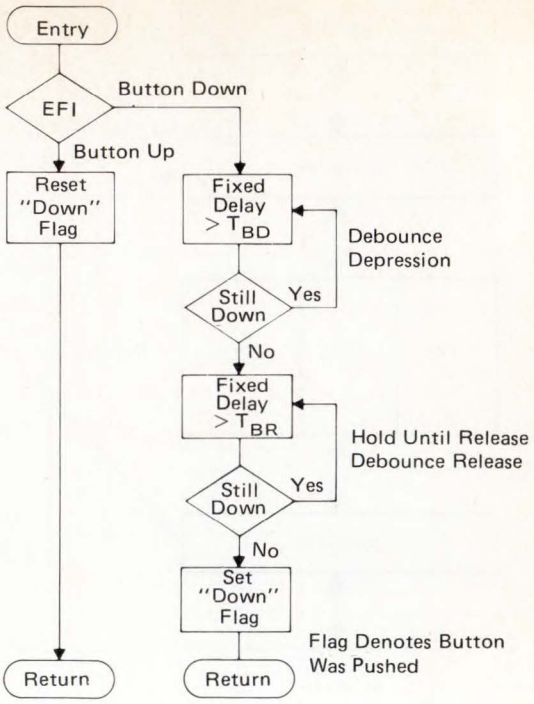


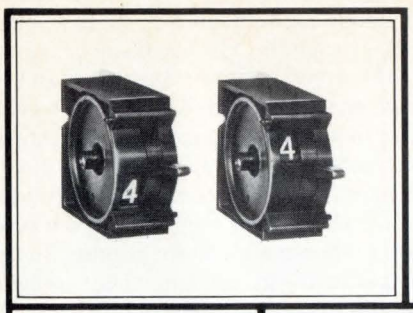
Fig. 10 Software debouncing subroutine tests to see if switch has been depressed and then later released. Method has drawbacks, though: it gives "switch down" input only upon release of switch, also wastes valuable time waiting.

readily handled, we will do so immediately. If not, the input will be saved for later when we have the time to handle it. Alternately, the processing associated with the input may be broken up into smaller computational blocks interspersed with refreshes of the display. These approaches are flowcharted in **Fig 4.**

Handling a dynamic display

How do you divide the processor's time between refreshing the display and doing the rest of its processing load? **Fig 5** shows a typical multiplexed display system and **Fig 6** gives the details on the display refresh rate. The minimum refresh rate for any digit should be 100 Hz. This is fast enough to prevent flicker under most stationary display conditions. The actual ON time of any digit is a compromise between the intensity of the display and the time remaining within the refresh period (T_R) for the processor to do some other work. It is desirable to minimize the display time (T_D) so that a maximum of processing time (T_P) is left for the rest of the processing load.

It is customary to overdrive multiplexed LED displays to increase their apparent brightness. The extent to which you can do this is a function of the duty cycle, T_D/T_R, of the display. This technique is not without its risks, however, for if the program crashes or hangs up someplace (because of a program bug, noise injected into the system, component failure, etc.) it is quite probable that a digit driver will be incinerated. You should be aware of this and take appropriate precautions, particularly when debugging your system. The segment information for a 7-segment display can be handled in either of two ways. If the data is in BCD, a device such as the CD4511, which contains a latch, BCD-to-7-segment decoder, and drivers, can be used as shown in **Fig 7**. A device such as the 7541 provides a similar function for hexadecimal displays.



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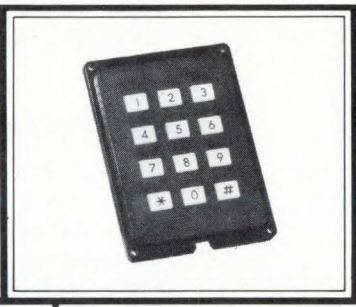

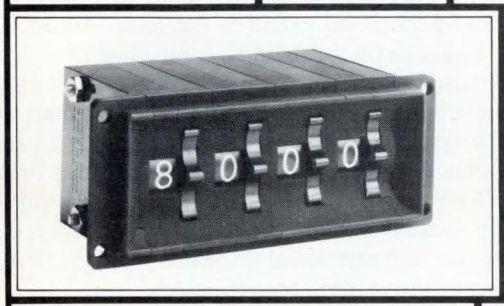

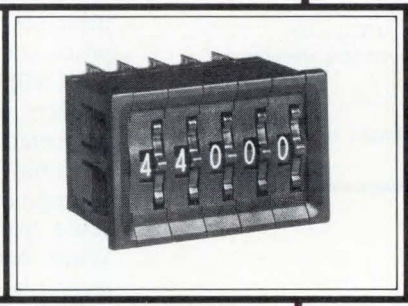

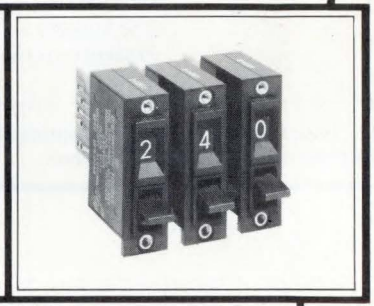

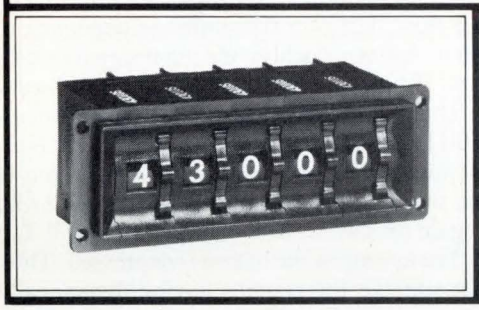

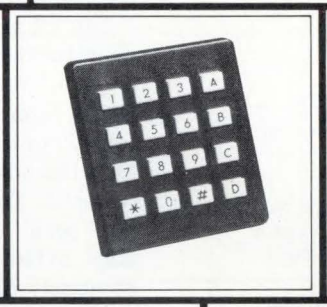

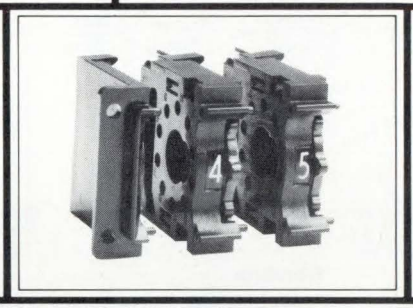

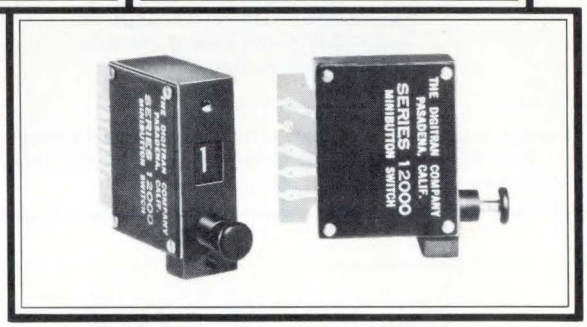

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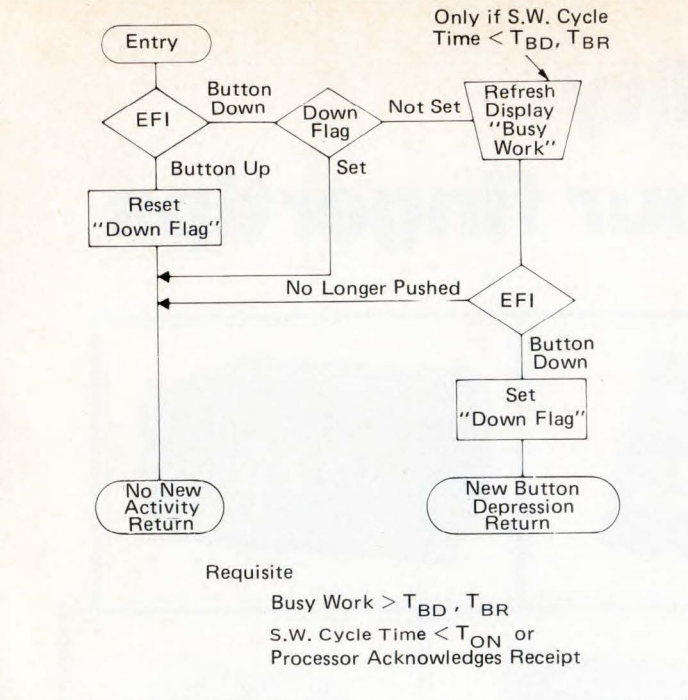

Fig. 11 Improved debouncing subroutine checks to see if switch is in same position as during previous look.

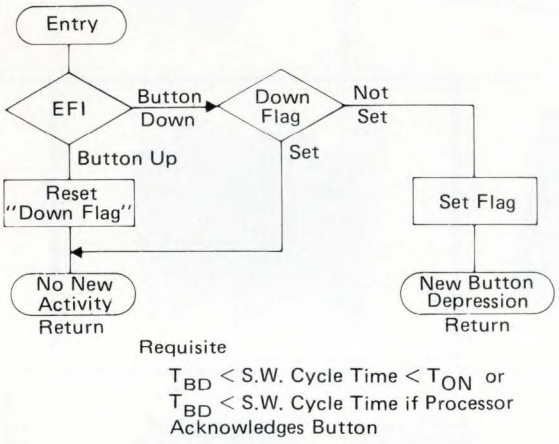

Fig. 12 Further improved debouncing subroutine has no timewasting loops. For method to work, cycle time must be greater than switch bounce time, but less than switch "on" time.

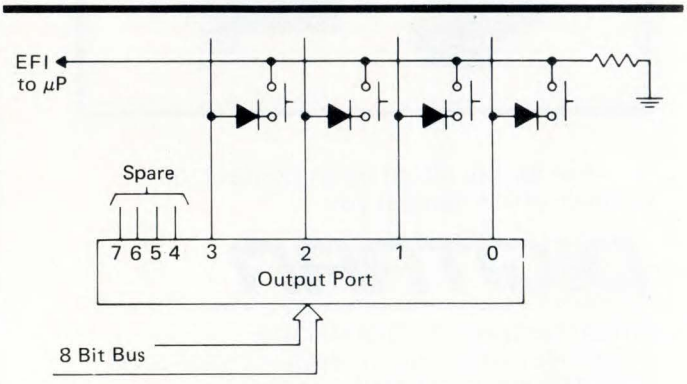

Fig. 13 Hardware for multiple-input scanning system. Fig. 14 gives software.

Or, instead of doing the code conversion in hardware, do it in software with a simple look-up table. With this software method, a less expensive simple output port can be used **(Fig 8)** instead of the MSI devices above. But, since I/O ports generally do not have enough drive to handle LEDs directly, an intermediate stage of buffering is necessary, defeating the apparent cost-effectiveness of this approach. No clear-cut distinction appears here, since factors such as the volume of the devices, cost of the I/O devices required by your processor, and type of display chosen all enter the picture. So far we have minimized output hardware and smoothed out the processing flow by multiplexing the input and display. Next, let's take a closer look at the input block and see what we find there.

Handling single-signal inputs

Software can even debounce switch inputs. First, consider a basic switch circuit shown in **Fig 9.** We shall assume a CDP1802 microprocessor having a flag input; the mechanical switch is shown attached directly to that input. It could just as well be a software-testable bit of an input port — the principles to be discussed would be the same. To signal the processor, a change on the flag line from a logic 1 to logic 0 level will be used. However, the mechanical switches tend to bounce, preventing a simplistic solution. The actual signal presented to the microprocessor will consist of three parts — an initial bounce, a stable ON period, and a release bounce. A program looking only for a simple 1 to 0 to 1 transition may sense many switch closures because of the bounce noise. While there are hardware solutions to this problem, software techniques may prove more cost-effective.

Fig 10 is a flowchart of a subroutine to debounce a mechanical switch. A test is made on the input signal to test for a switch closure. If none is found, a "switch down" software flag is reset. This flag may be some convenient bit in a CPU register or a bit in a RAM status word. If the switch is down, then the software will loop, waiting for the button to be released. The wait is performed to insure that the switch is not "seen" again for the initial bounce period $T_{BD} + T_{BR}$ and does, in fact, last as long as the button is depressed. Thus it is obviously not suitable for systems having dynamically refreshed displays. A further drawback, from the human-engineering standpoint, is that a response is made on the release of the switch rather than on its depression, the opposite of what one would normally expect. **Fig 11** shows a flowchart for an improved method that overcomes both of these drawbacks. Here, the subroutine that looks at the input signal remembers what that signal was the last time it looked; it then saves this information in a software flag we will call the "down flag." The routine operates as follows. If the button is now down and was also down during the last look, then the subroutine assumes that it is seeing the same button depression seen earlier. The subroutine then returns to the caller and indicates no new activity. If the button is not now down, but was during the last look, the subroutine assumes that the switch has been released, so it resets the "down flag" and returns to the caller, again indicating no new activity. (We are assuming the processor is only interested in switch depresions and not their duration.) But, if the switch is down now and was not down during the last look, this must be a new depression. The switch must be debounced, the "down flag" set, and a message returned to the caller. Notice in the flowchart that a second test was made after the delay generated in the "busy work" block. This is a debouncing technique that assures the switch has been in the same state for two successive samples before deciding on the true state of the switch.

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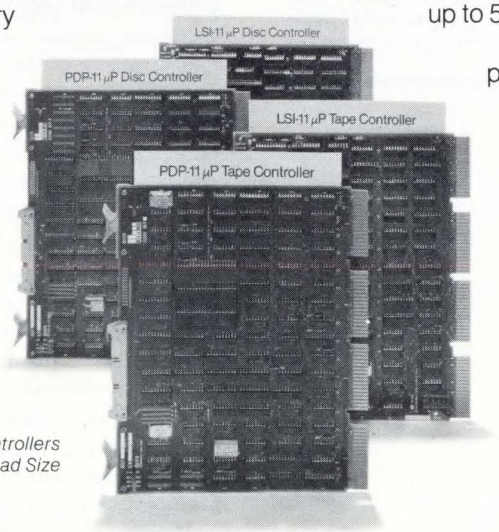

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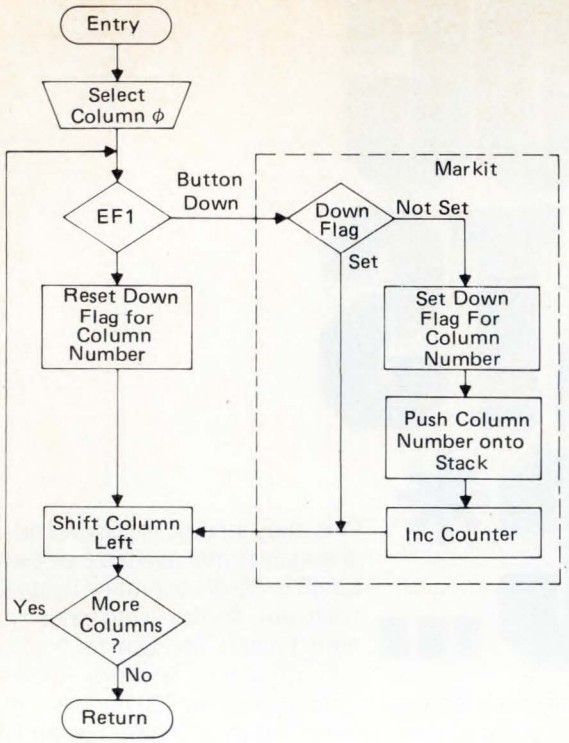

Fig. 14 Scanning subroutine looks for new switch closures and reports them to the main program by pushing the switch number onto a stack and incrementing a counter. Main program looks at counter to see if any new switch closures have occurred.

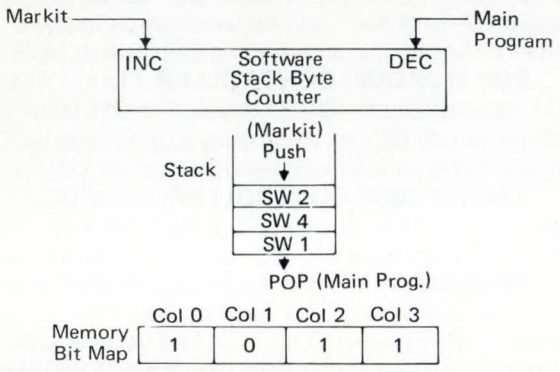

Fig. 15 Auxilliary portions of scanning subroutine. "Markit" portion of subroutine increments stack counter; main program decrements it. In example here, switches 1, 4 and 2 have been depressed.

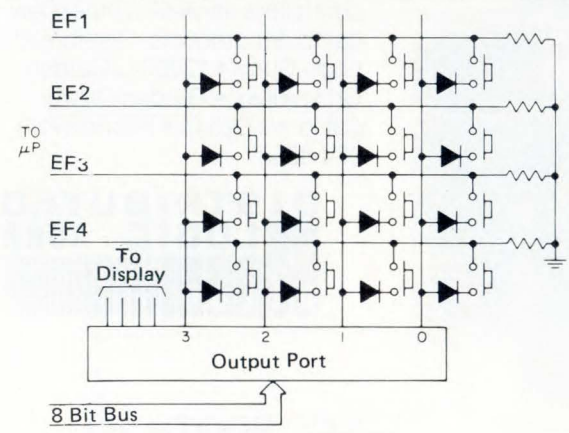

Fig. 16 Expanded scanning system for 16-key matrix.

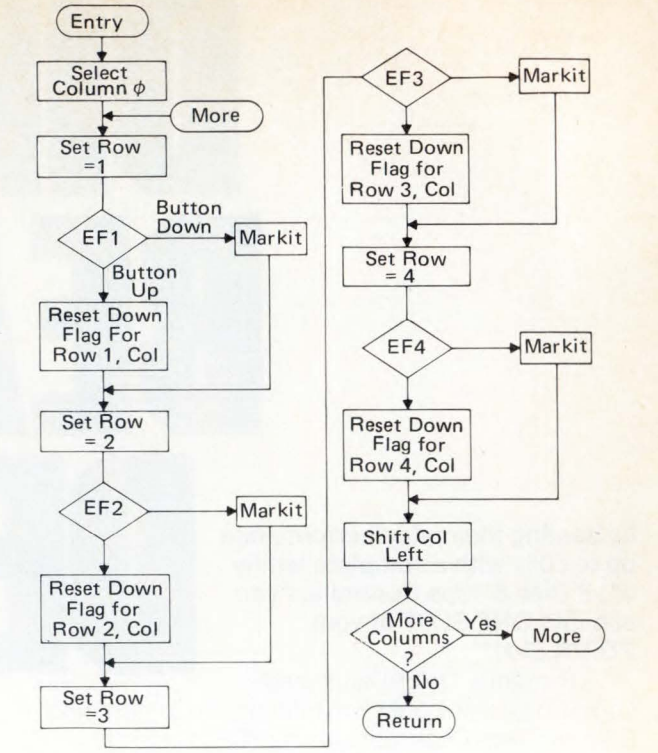

Fig. 17 Software for 16-key matrix scanning uses "Markit" subroutine for handling row as well as column information.

Additional constraints can lead to a better debouncing program. This program is waiting (and therefore wasting time) during the debounce period. If some additional constraints are placed on the software cycle time, however, the program can be further optimized. If the cycle time is greater than the bounce time (T_{BD}) but less than the switch ON time (T_{ON}), then the flowchart can be simplified to **Fig 12.** Here, there are no time-wasting loops, since switch bounce will effectively not be seen within the given timing restraints.

Scanning multiple inputs

A subroutine to handle four inputs by a scanning technique can be realized with the hardware of **Fig 13** and the flowchart of **Fig 14.** The software looks for new switch closures and reports any to the main program by pushing the switch number onto a stack and incrementing a counter. The main program will pop switch numbers off the stack and decrement the counter whenever the count is greater than zero. Let's take a close look at the flowchart and the auxiliary functions for the subroutine that is shown in **Fig 15.** We will assume that the timing constraints of **Fig 12** are met by this subroutine also, so that **Fig 14** is an extension of the basic flowchart previously developed. Upon entry into the subroutine, the first switch column is selected by outputting a 1 in bit position 0 of the data bus and examining the switch associated with that position. If a new depression is detected, the "down flag" is set for that switch (in the memory bit map), the column number is shifted and, if more columns remain to be scanned, the process is repeated. No switch closure or no new switch closure simply results in a column shift and continuation. When all columns have been scanned, the subroutine returns to the main program, which detects if any new switch closures have occurred by seeing if the counter has a value greater than zero. If so, the main progam will successively get a switch number from the stack and decrement the counter until it reaches zero. A section of the

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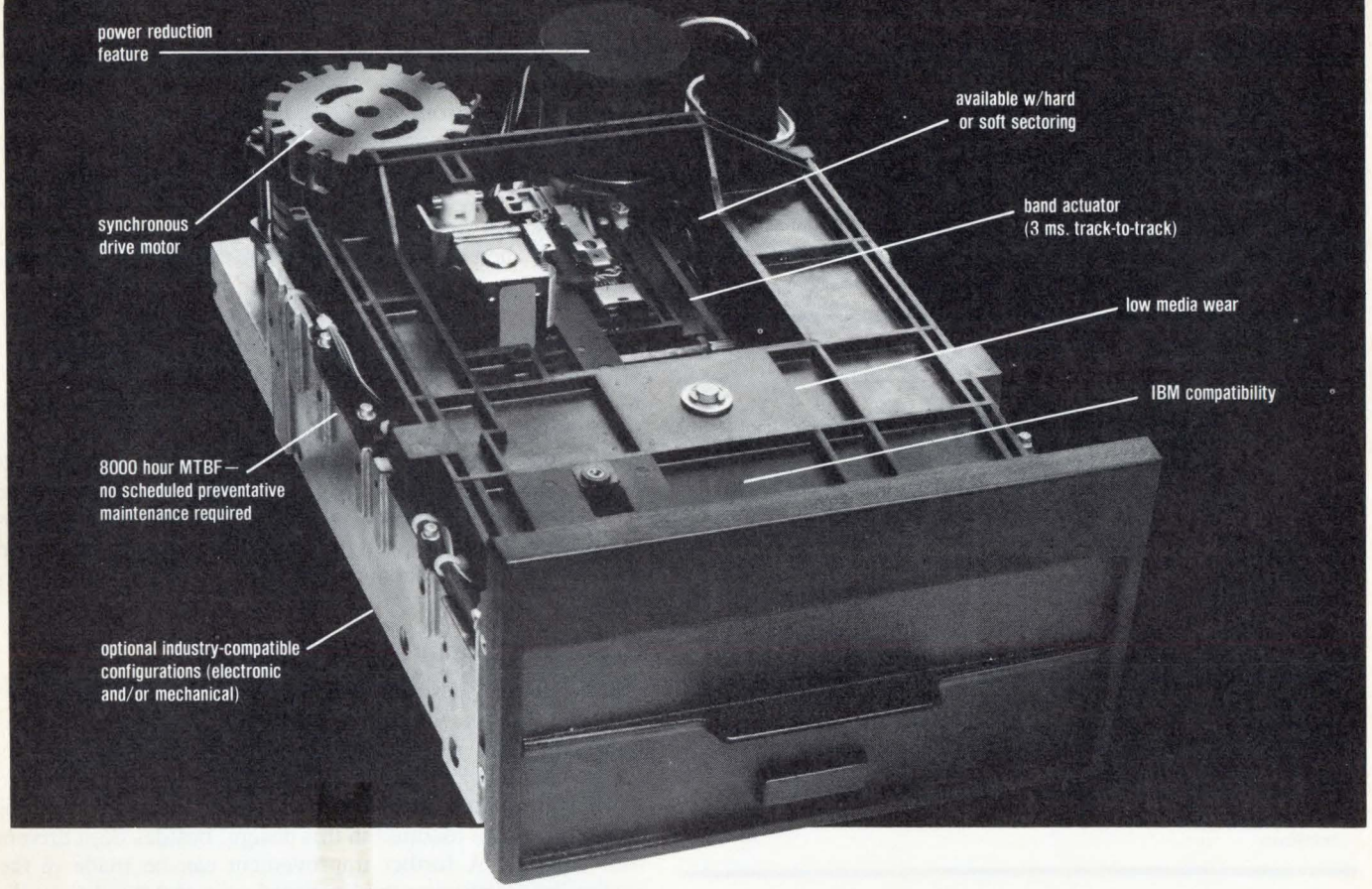

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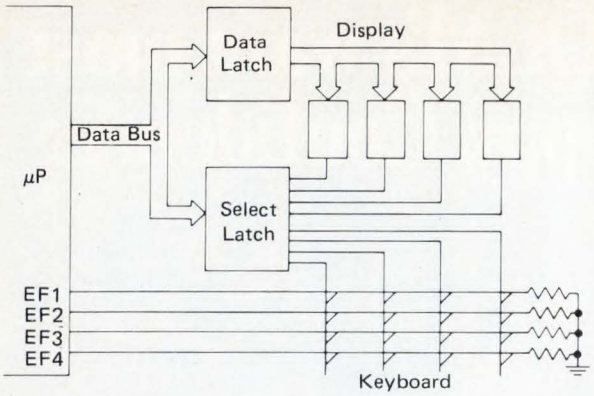

Fig. 18 Our original system with the component blocks filled. Using software has minimized the amount of hardware needed.

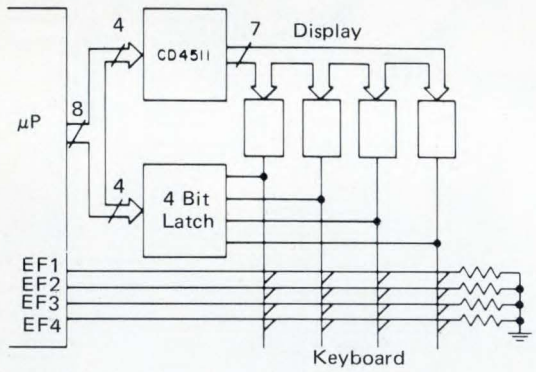

Fig. 19 Combining keyboard-scan and display-refresh signals produces smaller packages and cuts down on the number of output operations.

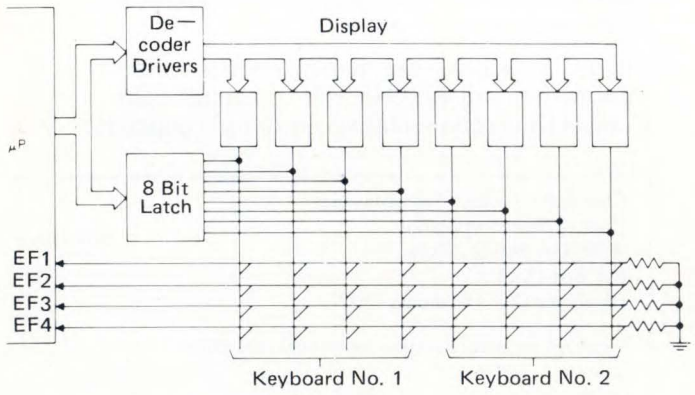

Fig. 20 Expanded system still uses only two ICs, but can scan two 16-key keyboards and an 8-digit display.

flowchart has been partitioned off and labeled "MARKIT," a common routine that can be used for an expanded keyboard scan routine discussed in the next section. Before we leave this section, notice that the approach taken above lends itself well to a multi-processor system in which one processor handles the keyboard scanning and puts key numbers in a stack accessible to other processors as well.

Keyboard scanning technique

The multiple-input techniques already described can be expanded into keyboard-reading software. Consider the arrangement shown in **Fig 16** for scanning a 16-key matrix. It is a simple extension of the arrangement just discussed. For a microprocessor having 4 input flag lines, such as the CD1802, the horizontal lines can go directly to the flat inputs as shown. For other microprocessors with a more limited I/0 structure, those lines could be brought in through an input port, but the principle of operation remains the same. **Fig 17** is a flowchart of the keyboard-scanning software where "MARKIT" is now responsible for handling row as well as column information. The basic interface between the maion program and keyboard scan subroutine remains the same; the subroutine places new key depressions on the stack, from whence they are passed to the main program. Notice that a key number's position on the stack does not necessarily represent when a given key was depressed with respect to the other keys on the stack, but merely reflects the order in which the keys were scanned. Since the stack is emptied on each cycle by the main program and only new key depressions are entered, two key numbers on the stack tells you only that both keys were down when the scan took place. To discriminate in time between rapid key depressions, a short software cycle time is necessary. But, remember that this time must be kept between the constraints of T_{BR}, T_{BD}, and T_{ON}. This technique has a limitation — the software does not tell the main program when a key has been released. Thus it cannot be used in a system requiring lockout of other keys when any one key is down.

Combined display and keyboard

Our original "classical" system has now been minimized to the point that it needs only two 8-bit output ports as additional hardware. The whole system of **Fig 1** is shown with its component blocks filled in on **Fig 18.** Our original objective to minimize hardware has been realized in that only two 8-bit output ports are required in this design, besides digit drivers (not shown). A further improvement can be made in the system by combining the keyboard scan and display multiplexing signals, as shown in **Fig 19.** Here a single-byte output is used, with the upper 4 bits being BCD-coded data for the display and the lower-order 4 bits used to simultaneously select a display digit and keyboard column. This arrangement does not reduce the parts count, but does give smaller packages if space is a consideration, and cuts down on the number of output operations and output bytes stored. A ready expansion of the system **Fig 20** still uses only two ICs, but can scan two 16-key keyboards and an 8-digit display.

Lowering system cost

We have shown that the hardware needed in a microprocessor-based system can be minimized by using software to perform functions that are usually done in hardware. The lower parts count should then produce a lower system cost. Of course, software isn't free — it takes time and money to develop and debug it. However, in volume applications, the spread-out cost of software development should be less than the replaced hardware, and the high-software system should also be more reliable. DD

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Purchasing Microcomputer Software Isn't Easy

The high cost of microcomputer software presents an obvious problem for many current and potential microprocessor users. Although the price of computing power (hardware) has decreased by several orders of magnitude over the past two decades, the cost of software has actually increased. Improved semiconductor technology now produces microprocessors and other complex computer circuits for a few dollars apiece. No similar revolution has occurred in software technology. It remains a very labor-intensive operation in an era of high labor costs and limited availability of trained personnel. Thus, you could easily spend $100,000 to write the software to run a $10 microprocessor. Furthermore, a development system (**Fig 1**) which can help with writing programs efficiently may cost $10,000 to $20,000. Even then, the quality, reliability and maintainabilty of the finished software may be questionable at best.

One solution to this problem involves purchasing software rather than producing it in-house. In this way, you would avoid the difficulties of expensive development, lack of qualified personnel, uncertain quality standards and complex scheduling (Ref 1-5). To help those who may choose to purchase soft-

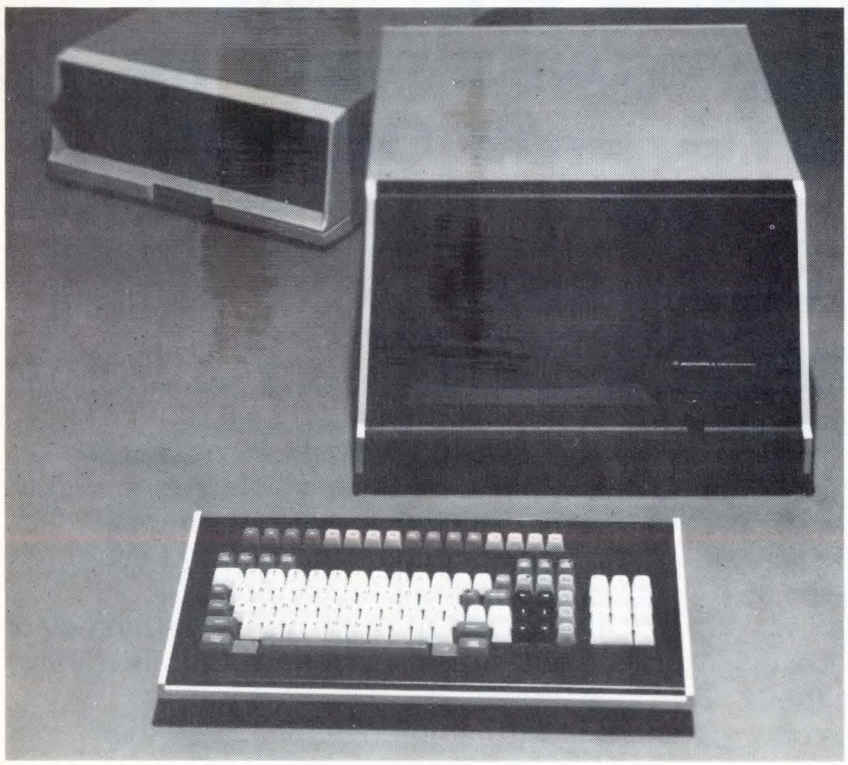

Fig 1 A typical microcomputer development system with its associated peripherals. (Courtesy of Motorola Semiconductor Products, Phoenix, AZ)

ware, we discuss the basic pitfalls in buying programs, what microcomputer software is actually available, and how you can judge that software. We briefly mention a few products and information sources.

The basic pitfalls

The very factors that make software difficult to develop also make it difficult to purchase. The most important factor is the lack of objective standards for evaluating software. How can you choose good programs when you are not exactly sure what makes a program "good"? No established standards for software testing (Reg 6), quality control, documentation or maintenance exist. We have even borrowed terms such as "testing", "reliability" and "maintenability" from the world of hardware. Most engineers are surprised to hear these words applied to computer programs and are quite uncertain as to their precise meanings.

A computer program is similar to a book, musical composition or work of art, for its development (and understanding) depends on complex thought processes that are difficult to judge objectively. We cannot measure a piece of software as we do a piece of hardware in terms of "revolution per second," "operating temperature range", "access time"

Fig 2 An advanced terminal with control functions and graphics capability. (Courtesy of Southwest Technical Products, San Antonio, TX.)

or "mean time between failures". Since software is so labor-intensive, little capital is required to enter the software business. Companies come and go, few establish a lasting reputation and none of them grow to the size and visibility of the leading hardware manufacturers. A software company faces the obvious problem of protecting its products, since no patents are possible and the copying of programs is a simple as the duplication of tapes or records. Vendor and buyer often relate to one another with mutual distrust and deliberate lack of communication.

All these problems clearly point to an end result. Most of the available software is very uncertain in quality, reliability and mantainability. Although a few ratings service, such as Datapro and the Association of Small Computer Users, attempt to provide objective evaluations, they do not presently rate all products. The viability and integrity of many software companies is extremely questionable. Even though some firms can write and market good software, the buyer faces the very difficult problem of identifying, obtaining and using it.

Available Microcomputer Software

We can divide the available software

into these two categories:

- Systems software (such as operating systems, assemblers, editors, compilers, debuggers, utilities, I/O drivers, diagnostics and loaders) which simplifies system operation and makes software development faster and easier, but does not perform any applications task
- applications software which performs the actual production work. This division is rough, because

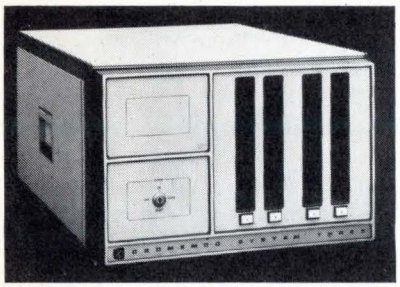

Fig 3 An expanded microcomputer system. (Courtesy of Cromemco, Mountain View, CA.)

some system software is designed for specific applications. The user may only need make a few modifications to handle common situations. On the other hand, some application software may be packaged with the system's software that makes it run.

In general, the market for microcomputer system software is far more developed than the application software market. Many companies produce operating systems, assemblers, editors, compilers, debuggers, utilities, I/O drivers, diagnostics and loaders. Of course, they produce this software most commonly for the popular microprocessors, such as the Intel 8080 and 8085, Motorola 6800, Zilog Z-80 and MOS Technology 6502. Some typical examples of this software include the CP/M operating system and associated programs available from Digital Research (Pacific Grove, CA.) for 8080/Z80-based microcomputers, the MTOS Multi-Tasking Operating System available from Industrial Programming (Greenvale, NY) for 8080/6800 systems, and the FORTH language available from Forth, Inc. (Manhattan Beach, CA.) for a variety of microprocessors. A leading vendor of assemblers, compilers and other software for many microprocessors in MicroSoft (Bellevue, WA). Many other vendors also supply products in this area; we have mentioned only a few of the leaders.

Little application software is available. Perhaps the most common engineering software products, mathematical packages, perform floating point arithmetic and a few basic functions. Some vendors may offer occasionally other mathematical procedures, such as matrix inversion, root finding, fast Fourier transform and digital filters. At the present time, most common application software falls outside the engineering area — in games, demonstration programs and basic business functions, such as accounts payable, accounts receivable, general ledger and payroll. Clearly, the reasons for this limited development lie in the difficulty of producing general application software, the wide range of applications, the limited markets and the problems of proprietary methods and information. Undoubtably application software will be-

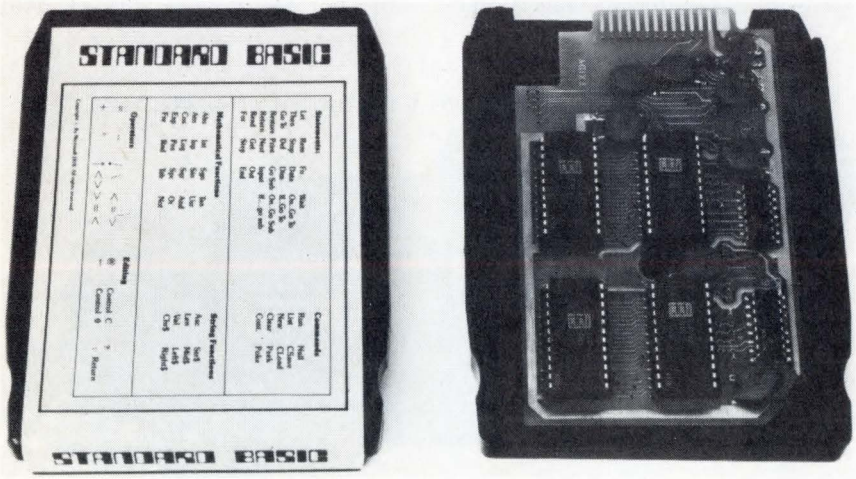

Fig 4 Standard BASIC in ROM-PACK for the Exidy Sorcerer. (Courtesy of Exidy, Data Products Div., Sunnyvale, CA)

come available, but its quantity will remain limited and its cost will stay relatively high. Most of it will be usable only on popular microprocessors and in common applications. Otherwise, the only way to buy application software will involve hiring a consultant to write it. Although consultants can draw on their previous experience, the old programs that they may supply are likely to be very specific or proprietary to other clients.

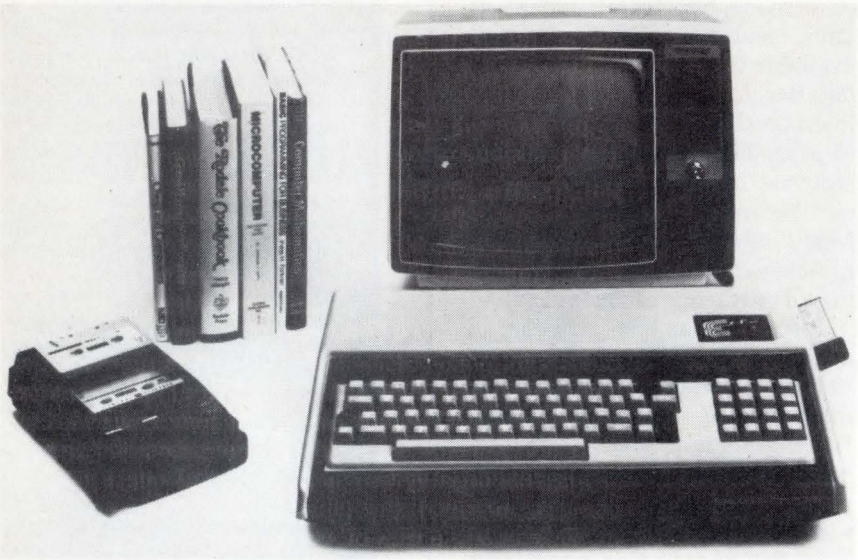

Fig 5 The exidy Sorcerer computer with a ROM-PACK plugged into the side. (Courtesy of Exidy, Data Products Div., Sunnyvale, CA)

Judging software

Evaluating a computer program depends on many factors, such as the following:

- Will it run on your computer? If not, a modification that is advertised as simple may turn out to be a major task. The vendor can easily modify a well-written program, but user modification is generally difficult.
- Is it suited to your application? Consider only those factors important for your application. Remember that it makes no sense to pay for speed or accuracy that you will never use; no program is a better buy, because it does a large number of things in which you have no interest.
- How fast does it run?
- How much data can it handle?
- How much memory does it require?
- What peripherals does it require? Since the software cannot instruct the hardware to do things beyond its capabilities, functions that depend on nonexistent capabilities will simply be inoperative. On the other hand, some software may require a particular type of terminal, printer or disk to run at all. For example, some editors can use a simple video monitor, while others need a complete terminal with control functions and graphics capability **(Fig 2)**.
- What other software does it require? This need may include a specific operating system, compiler or interpreter, loader or editor.
- How easy is it to use? Although often a subjective factor, ease of use certainly depends on how simple the input procedures are, how clearly the outputs are identified, and how well-suited the documentation and usage is to a particular application.
- What error detection, correction and recovery procedures does it implement?
- How portable is it? Some programs can only run in one specific configuration of a given computer; others are more easily modified.
- Can it be reconfigured for an upgraded system? The most common type of change embodies improving the system to support a new or better printer, more memory or a new or larger disk. Some programs allow such modifications with ease, while others require a major reworking. Some of the newest computers **(Fig 3)** can offer impressive advantages in speed and storage capabilities; software that you bought for an earlier system should be compatible with the upgraded system.
- How much does it cost? What do you get for your money? Some questions to consider here should at least encompass whether source code is included, how long the license (if any) lasts, whether a single use is covered, whether you must pay a royalty on resale.
- In what medium is the program available? Clearly, the medium must be compatible with your system. For example, an Exidy Rom-Pack **(Fig 4)** will fit right into a Sorcerer computer **(Fig 5)**, though it would be useless with any other machine. A program that is only available on a medium that your system cannot use or that is not compatible will result in endless headaches. Few conversion programs exist and finding suitable hardware for conversion is a difficult problem. Be especially careful of cassettes **(Fig 6)** and floppy disks **(Fig 7)**; both

Fig 6 Product line of cassette tapes.

Fig 7 One type of minifloppy diskette of those available in a variety of forms for different computers. (Courtesy of Verbatim, Sunnyvale, CA.)

types of drives use many different and incompatible recording standards.

- What standard does the program use? They may include a standard computer language or popular operating system.
- What documentation does it provide? The documentation may include manuals, program listings, user guides and flowcharts.
- Is maintenance provided or offered at extra cost? How will new versions and corrections be distributed?
- What agreements must you sign to use the software (i.e., non-disclosure)?
- Is there a warranty? What happens if the program will not load into your system or does not work?
- Have you checked the experience of other users of the software package? Again, we note the availability of rating services for collecting user evaluations. If the raters do not provide adequate information, you may ask the vendor to direct you to a nearby purchaser of the same package.
- What is the vendor's record? How long has he been in business? What is his record for service? Is he likely to continue in business?
- Is the program available? Many advertised products (including hardware) offer little more than vendor's imagination and clever promotion. The vendor may even be using the response to the publicity to decide whether he should develop the product or obtain financing.
- Does the program conform to good programming practices? It should follow the rules of top-down design, modular programming and structured programming (Ref 7-10). A program that follows these rules makes the product easier to use and maintain.

Many of the questions just presented are the same ones that you would ask when investigating any uncertain choice, regardless of the product being purchased. When considering an unknown vendor, you may wish to try his wares by making a small purchase as a check on product quality and response time.

Conclusion

Without question, the purchase of software makes economic sense, because the cost and difficulty of developing software shows no signs of decreasing. However, the very problems that make software difficult to develop also make it difficult to purchase. The buyer will find the world of software a highly uncertain one, since vendors and products are doubtful in quality and reliability. The importance of software in most systems means that buyers must evaluate their purchases carefully. Although new and improved ratings services and better-known and more established vendors will emerge, the purchase of software will continue to pose difficult problems during the next year or two.

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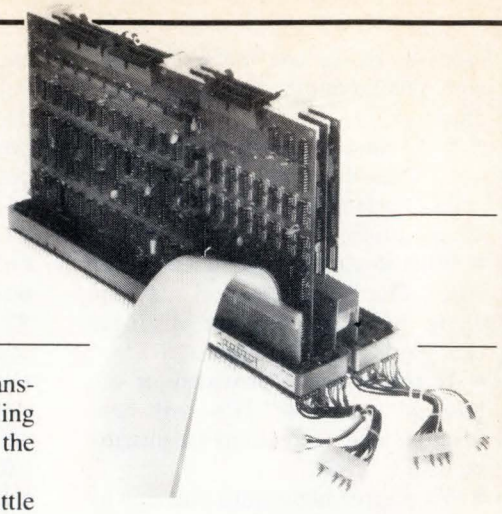
PRODUCT HIGHLIGHT

PDP-11 Synch/Asynch Communications



Multiplexer Offers Full DV11 Software Compatibility

An improved synchronous/asynchronous communications multiplexer for the full family of PDP-11 computers, the DV/16 ABLE multiplexer, provides several advantages over the DEC DV11 and full compatibility with all DEC DV11-related software and incorporates a novel design offering greater application flexibility, improved performance and smaller size than the DV11.

While the DEC DV11 provides 8 or 16 communication lines with synchronous or asynchronous lines, which must be purchased in fixed groups of four lines, the DV/16 offers a choice of 8, 16, 24 or 32 communication lines with both synchronous and asynchronous operation in user-selectable groups of four lines. They are also smaller — the 16 line DEC DV11 occupies nine slots in a dedicated backplane, while ABLE's comparable DV/16 is comprised of only four PCBs which may be installed in any 4 contiguous SPC slots. Users requiring 32 lines would need to order two DV11's from DEC which would require 18 slots and two backplanes; the 32 line DV/16 equivalent from ABLE requires only seven SPC slots. Certain applications which cannot use the DEC DV11 due to over-saturation of the Unibus will find the DV/16 particularly attractive since it transfers words rather than bytes, doubling the transfer rate and thus freeing the Unibus for other devices.

The DV11 user is offered little choice: he may opt for all synchronous operation, all asynchronous operation, or four lines of each (but he may not choose which four lines). Once he has made his selection, it is final, he cannot alter it (without replacement) even though his needs change in the future. To solve this problem, we decided to utilize the more flexible USART rather than UART inherent to the DEC DV11 design. With the USART we could offer switch selection of synchronous and asynchronous operation in groups of four lines and as a bonus, we attained the added versatility of internal baud rate selection.

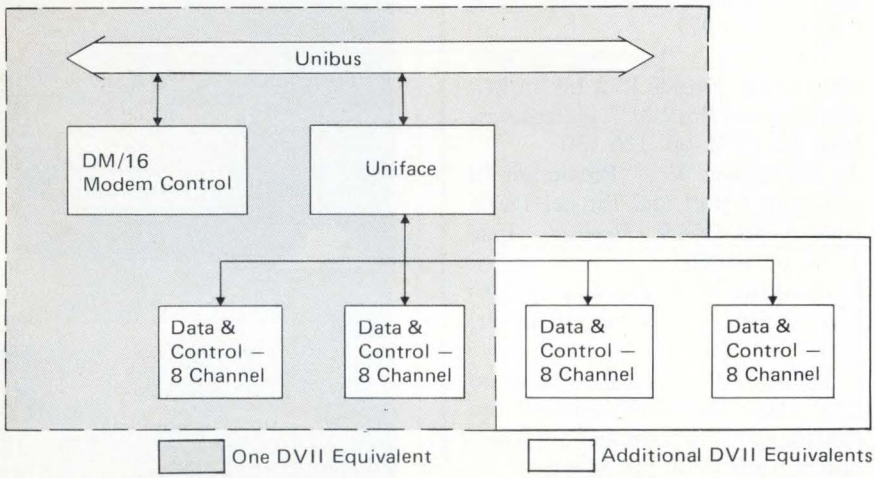


Fig 1 DV/16 Simplified Block Diagram

The second problem we attacked is the Unibus time required by the DV11 to transfer information. With two DV11's on the PDP-11/45, for example, the Unibus can quickly become too saturated to accommodate disc storage. We felt we could decrease saturation of the Unibus and speed data transfer by handling data word-by-word rather than byte-by-byte. So, instead of reading each word twice to transfer the two bytes, we chose to read the word and then buffer it so that the second byte wold be ready after transmission of the first byte. The result doubles the rate of data transfer or, put another way, uses half the Unibus bandwidth required for DEC DV11 operation.

The DV/16 is more compact than the DV11 (saves user backplane space). By placing all Unibus interface functions on one board, it would need only one board for each 8 USARTS and one for the modem. This convenient package allows users to choose the number of channels in increments of 8 and opt to exclude modem control if unneeded. The universal/Unibus interface, UNIFACE™, is an intelligent processor providing DMA and interrupt facilities and communications with I/O cards via a 20-bit microbus called the ACTbus.

The UNIFACE card should also impact future designs. The microprogrammable interface can be reprogrammed for other controller designs with separate "personality modules" added to perform I/O functions for each application.

An additional advantage brought about by UNIFACE is the further enhancement of ABLE DV/16 by adding a dual port memory to speed processing of protocol handlers and free Unibus from time required to fetch protocol tables. In this design, memory would have ports onto both Unibus and ACTbus. In accessing a protocol handler, DV/16 would use its own internal microbus rather than generating an interrupt on Unibus, thus optimizing Unibus availability for other system functions.

Able Computer Marketing, 1751 Langley Ave., Box 17779, Irvine, CA 92713. (714) 979-7030**Circle 260**

NEW PRODUCTS

DYNAMIC GRAPHICS SYSTEMS

The Wizzard 7000 and 5000 families comprise graphic peripherals, graphic terminals, and stand-alone graphic processing systems. The Whizzard 7000 series features an improved vector generator using a proprietary technique, Adaptive Timing; an advanced 32-bit tri-state graphics bus; and a proprietary 32-bit bipolar μP. Also with the 7000 family are three dimensional rotation and an optional color monitor. The 7000's dynamic graphic systems allow both 2D and 3D simultaneously on the same display. Four colors are standard, with an optional fifth color available. For Nova of Eclipse owners, the Whizzard 5000 family is said to offer the lowest-cost, high-performance interactive graphics in today's market. A total refresh graphic system, the 5000 offers selective erase, translation, rotation, scaling and zoom, and places emphasis

on remote graphics processing. The Whizzard 5000 is available as a stand-alone processor, RS232 communicating terminal or dual board MG552 processor fo installation within a customer's Nova or Eclipse computer. Dynamic Whizzrd 5014 systems are designed to easily replace and be upward compatible with the Textronix 4014 series of storage tube terminals. **Megatek Corp.,** 3931 Sorrento Valley Blvd., San Diego, CA 92121. **Circle 243**

8-BIT mP WITH 16-BIT ARCHITECTURE

The 8088, said to be the world's highest performance 8-bit μP contains the 16-bit internal architecture of the 8086 combined with the 8-bit bus interface of the 8085A. The 8088 is 100 percent software compatible with the 8086. It features advanced arithmetic and alphanumeric (ASCII) data capabilities so that programs require fewer instructions and run faster than with other 8-bit machines. The internal architecture of the 8088 is essentially the same as the 8086. It has all the features found in that 16-bit unit including capabilities not found in any other 8-bit μP: byte addressing; flexible addressing modes — two levels of indexing plus displacement possible in a single operation; 8/16-bit hardware multiply/divide, signed or unsigned; extensive string handling instructions; instruction look ahead; and dynamic program relocation capabilities. **Intel Corp.,** 3065 Bowers Ave., Santa Clara, CA 95051. **Circle 240**

PDP-11/70 ADD-IN MEMORY

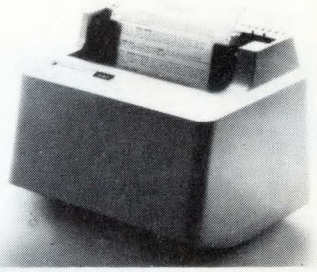
Pincomm 70s semiconductor module is pin-compatible with DECs PDP-11/70 using DEC's memory chassis with no modification required to existing DEC hardware. Memory card capacity is 256K bytes (64K × 32 + 7 ECC). Up to 16 PINCOMM 70s and/or DEC memory cards can be installed in the MK-11 chassis. $4985. **Trendata,** 3400 W. Segerstrom, Santa Ana, 92704. **Circle 236**

LOW-COST PRINTER

Printout of exceptional quality is achieved on a new, $560 end user price, non-impact printer. Alphanumeric images in the full 96-character ASCII set, with upper and true lower case, are delivered by the Comprint 912. The 9×12 printhead matrix generates overlapping dots to create more fully formed characters. The Comprint unit writes 80-column lines at 225 characters/second (170 lpm) — on 8 ½'' wide paper. IEEE-488 and strobe/acknowledge are supplied with the parallel-interface model; RS-232C and 20-MA current loop are available on the serial-interface model priced at $39 more. A six-month warranty is offered on the Model 912. The printer weighs under 15 pounds, and measures 15-¼'' W × 13-½'' L × 5-¾''H. **Computer Printers International, Inc.,** 280 Polaris Street, Mountain View, CA 94043 **Circle 255**

IMPACT PRINTER

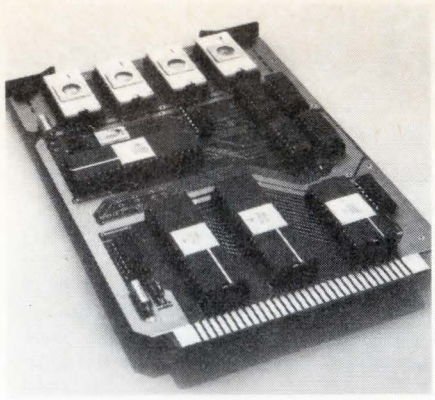
IDS 440, minimizes hardware and increases flexibility because the μP controls everything. The 20 lb. unit's only PCB contains the supply, M3870, additional buffer memory, solenoid drivers, print head drivers, stepper motor drivers for the paper feed, all switches, indicators, paper-out sensor and EIA cable connector. Specs include: char. format, 7×7 dot matrix, 0.110'' high; char. set, full ASCII u & l case; char.



densities, 8.3, 10, 12, 16.5 cpi and enhanced double width; printing speed, 100, 120, 144, 198 char/sec unidirectional; paper drive, tractor feed stepper motor driven, max. slew rate of 3.5 ips; maximum line length, 73, 80, 96, 134 char. at 8.3, 10, 13, 16.5 cpi; paper width, 1.75 - 9.5''; line spacing, switch selectable 6 or 8 lpi. **Integral Data Systems,** 14 Tech Circle, Natick, Mass. 01760. **Circle 239**

NEW PRODUCTS

SINGLE BOARD COMPUTER



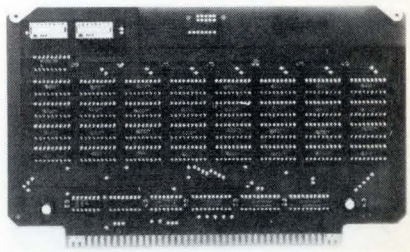
The model 1050 single board computer is aimed at intelligent, process control/monitoring applications. It provides high-reliability with adaptable computing power on a 4 1/2" by 6 1/2" printed circuit board requiring only +5V. This stand alone computer is designed around the Motorola 6802 microprocessor and contains 128 bytes of RAM, operating at either 1 or 2 MHz using an on-board crystal controlled clock. An additional 2K bytes of RAM and 8K bytes of EPROM can be loaded on the board. $250. **Adaptive Science Corp.**, 4700 San Pablo Ave., Emeryville, CA 94608. **Circle 197**

EXPAND COMPUTER STORAGE

Application note describes how computer owners (OEM or end user) can easily expand their available computer memory by adding Digital Data Systems add-on memory systems. Up to 512K × 20 of core or semiconductor memory is available in 5 1/4" or 10 1/2" high 19" rack mountable, self contained chassis. Paper describes how the system can be interfaced to any computer, communication between the existing and add-on memory, limitations on maximum storage, how to order, etc. It also provides general information about add-on memory systems. **Digital Data Systems Inc.**, 1396 N.W. 65th Terrace, Plantation, FLA 33313. **Circle 257**

EXORCISER COMPATIBLE 16K RAM

The 9627 is a 16Kbyte static RAM module. This module is configured as two independent 8K blocks which can be individually placed at any 8K boundary in the memory map. The 9627 is available in the standard configuration with 480



ns access time. Power required is a single 5V supply at 1.7 A. The 9627A, a 300 ns version is available on special order. 9627: $495.00; 9627A: $595.00; 9627-8: $295.00. **Creative Micro Systems,** 11642-8 Knott Ave., Garden Grove, CA 92641. **Circle 206**

FIBER OPTIC MODEMS

Three off-the-shelf electro-optic digital modems that fulfill a broad range of data communication requirements include: the CEO-M-O6M — a full duplex asynchronous TTL compatible unit for transferring serial data at bit rates from dc to 6Mbit/s with a maximum link loss of 12 dB; — the model CEO-M-300K — transfers serial data at bit rates from dc to 300Kbit/s with a maximum link loss of 22 dB; — and the CEO-M-56 — RS-232C compatible optical modem is a full duplex synchronous unit with link loss capability of up to 35 dB at bit rates of 28 and 56Kbit/s. The transmitter of these modems employs a high radiance LED source while the receiver uses a PIN photo diode detector. These digital transmission systems offer full duplex communications capability with the inherent advantages of fiber optics: freedom from EMI & RFI; immunity from groundloop problems; high data integrity (BER=10^{-9}); and security from tapping or interference. **Constar Communications,** 1240 Ellsmere Rd., Scarborough, Ontario, Canada MIP 2X4. **Circle 199**

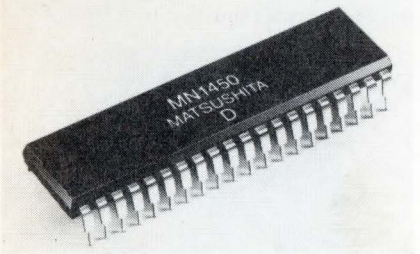
BI-SYNC-ASYNC SERIAL CONVERTER

A bi-sync-to-async serial converter capable of interfacing an EBCIDIC binary synchronous host or terminal with any serial RS-232C ASCII device or with a teleprinter comes in two configurations. The Model BAX-1-80 is compatible with 2780/3780

devices for batch operation. Model BAX-1-75 is compatible with the IBM 3275. Both employ IBM-type communication terminals and perform all buffering and real time requirements of protocol. Standard featues of the devices include: synchronous speeds up to 4800 baud and asynchronous speeds up to 9600 baud; automatic code conversion; controls for asynchronous baud rates and mode selection; an EBCIDIC transparency mode; automatic record blocking and de-blocking; and loop back self-test/diagnostics. Several options also are available. **Alphamatrix, Inc.,** 1021 Millcreek Dr., Feasterville, PA 19047. **Circle 137**

ULTRA-LOW POWER CMOS μC

A single-chip, low-power (2 mW typical) CMOS 4-bit μC, designated as "MN1450", is a low-power version of the previously introduced MN1400. It comes in a 40-pin standard plastic DIP offering a number of "on-chip" functions. These include the ALU, 1024 x 8 ROM, 64 x 4 data RAM with 4 words that are directly addressable, 8-bit counter/timer, two 5-bit parallel input ports



and two sense lines, one 5-bit parallel (with latch) output port, 8-bit PLA, (programmable logic array), one 12-bit discrete output port. The MN1450 offers a 75-instruction instruction set, a 10 μS cycle time, and operates from a single +5 Vdc power supply. Its I/O is fully TTL compatible. **Panasonic,** 1 Panasonic Way, Secaucus, NJ 07094. **Circle 133**

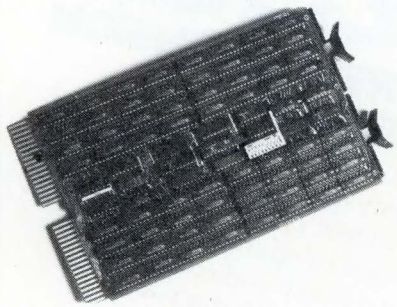
LIMITED DISTANCE MODEM

The LDM-7296's limited distance modem operates over distances up to 5 miles on standard cables at synchronous data rates from 1800 to 9600 bps, or asynchronous at 0 to 9600 bps. The modem provides both transmit and receive clock plus an "instant sync" feature, activated by carrier detector, that is ideal for use in multipoint polled applications. The modem also provides a full EIA interface, a complete status display, and both analog and digital loopback switches. It is available as a stand-alone en-

closure, a ten channel rack-mounted unit, or as a single circuit card assembly 6 x 13". **Syntech Corp.,** 11810 Parklawn Dr., Rockville, MD 20852. **Circle 152**

LSI 11 STATIC MEMORY

The VML 1116 semiconductor memory is hardware and software compatible with the



LSI 11, LSI 11/2 and PDP 11/03 computers. The memory has 16K x 16 on a single dual width P.C. board. On board DIP switch allows memory operation to 124K. The 4K × 1 NMOS Static RAM design eliminates the need for refresh. A single +5 VDC @ 2.5 amps, per 16K derived from the bus option slot is all that is required. Memory access time is 250 ns and cycle time is 350 ns. **Computer Extension Systems, Inc.,** 17511 El Camino Real, Houston, TX, 77508. **Circle 129**

D/A BOARDS FOR LSI-11

The ST-LSI-DA 4-channel stand alone D/A PC boards slide into and interface directly with Digital Equipment Corp.'s LSI-11 μC. These analog output peripherals with jumper-selectable addresses can be cascaded indefinitely. Channel expansion is limited only by the LSI-11's memory capacity and the number of available card slots on the μC data bus. Features include four full scale output voltage ranges: 0 to +5, 0 to +10, −5 to +5, and −10 to +10 volts. Input digital coding is straight or offset binary, or 2's complement. Each ST-LSI-DA4 is available on a half-quad-size PC board (8.5 x 5"). The ST-LSI-DA4A is available with an on-board optional ±15 DC/DC converter that draws its power from the LSI-11's 5V bus at a 1A maximum current drain. The ST-LSI-DA4B model omits the DC/DC converter and requires an external ±15V at 150 mA for operation. ST-LSI-DA4A, $535; ST-LSI-DA4B, $475. **Datel Systems, Inc.,** 11 Cabot Blvd., Mansfield, MA 02048. **Circle 148**

NEW PRODUCTS

PARALLEL OUTPUT PRINTER INTERFACE

Developed for use with Centronics high speed draft printers and Digital Equipment Corp.'s Decstation-78 series of computer systems, the CI/78-A interface is designed to operate from the parallel output port on the VT/78 video data processor. The manufacturer claims this is the first time that a commercially available interface has been produced that will allow another manufacturer's printer to operate on this series of DEC hardware, with parallel data output. $395. **Computer Interactions, Inc., P.O. Box 1354,** Roslyn Heights, NY 11577. **Circle 175**

BASIC FOR TEKTRONIX

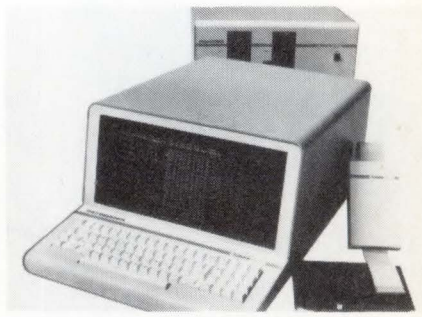
An enhanced Basic language compiler, designed for the Tektronix 8002A microprocessor development lab (MDL), allows full program development for the Intel 8080A and 8085A μP as well as the 8080 subset of instructions for the Zilog Z-80. Tektronix 8002A MDL Basic incorporates a number of optimizing features that conserve memory and reduce run time. For example, a program may be written in several modules which can then be compiled separately and combined using the 8002A linker. The USES and PROVIDES statements allow the modules, which may be either assembly language or Basic, to communicate with each other. The USES and PROVIDES statements also make it possible for the programmer to specify which procedures should be called when an interrupt occurs, and which variables are associated with I/O ports or absolute memory addresses. $950. **Tektronix,** P.O. Box 500, Beaverton, OR 97077. **Circle 185**

ONE-CHIP TIMER/CONTROLLER

The TMS 1121 features 18 daily or weekly selectable timer settings, four independent switched outputs for control of external devices, 50 Hz or 60 Hz line synchronization, and display signal driver input for both day of the week and time of the day. When the universal timer/controller is connected to a keyboard, drivers, an LED display, and a single 9-volt power supply, the combination forms an accurate low-cost timer control module. The TMS 1121 is offered in a 28-pin plastic DIP. $8.61 (100). **Texas Instruments Inc.,** P.O. Box 1443 M/S 6406, Houston, TX 77001. **Circle 177**

UNIVERSAL DEVELOPMENT SYSTEM

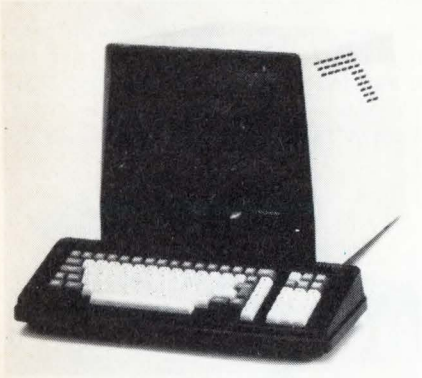
The AMDS-AFD, is said to provide all the development tools needed for 8080, 8085, 6800, 6802 or Z80 μP-based product design and test. The central element in the package is Futuredata's AMDS – the CPU (with choice of processor and 48K bytes of static RAM), universal logic analyzer, CRT and keyboard are all integrated into the compact AMDS station. Hardware development capabilities of the AMDS-AFD system include real time incircuit emulation to 5 MHz; 48



channel logic analyzer with 256-state trace buffer, three hardware break registers, loop counters and delay counters; dual, double density disk drives with one Mbyte storage capacity and a high speed (over 20,000 cps), high resolution 24 x 80 CRT display. A software development set on diskette includes relocatable macro-assembler, object program linker, screen-based editor, interactive debugger with disassembly and symbolic debugging and command control language. $16,500 (includes choice of 8 bit processor: 8080, 8085, 6800, 6802 or Z80). **Futuredata Computer Corp.,** 11205 S. La Cienga Blvd., Los Angeles, CA 90045. **Circle146**

SMART APL TERMINAL

The Model 11 APL/ASCII unit may be used either in conventional interactive (character) mode or in block mode for editing and forms-filling. In APL, it displays all APL characters and overstrike combinations, as well as alphanumerics. When sequenced into ASCII, it displays 96 ASCII characters (plus 32 control codes in Monitor mode.)"Instant replay" allows viewing of either overstrike character separately. In either APL or ASCII mode, it will store (keyboard-entered or computer-loaded) up to 32 programmed functions — forms, answerbacks, control sequences — totalling more than 500 characters. $1,590.00. **Teleray Division,** Research, Inc., P.O. Box 24064, Minneapolis, MN 55424



Circle 211

BUSINESS COMPUTER WITH TURN-KEY APPLICATIONS SOFTWARE

The Compucorp 625 Mark II is offered with an extended Basic language operating system and up to 64k bytes of internal memory. In a single package, not much larger that a typewriter, this computer incorporates the display, memory and hard-copy peripherals. With the complete array of controllers available with the 625 Mark II, the computer can also be interfaced to a wide range of external printers, plotters and other devices. In addition, several special controllers allow the computer to be used for data acquisition and other scientific real-time applications. **Compucorp,** 1901 S. Bundy Dr., Los Angeles, CA 90025.

Circle 189

PRINTERS AND PRINTER/PLOTTERS

Printing speeds for 3200A printer/plotters and 3250 printers has increased from 500 to 1000 lines per minute. These models, available in rack-mountable or desktop versions, are said to offer the fastest printing speed of any high resolution (200 dot-per-inch) electrostatic printer. Printing a

64-line, 11" by 8 1/2" page in 3.9 seconds, they deliver up to 15 cut pages per minute. The two models print 1000 132-column lines per minute with 12.5 characters per inch. They print 64 lines per 11" by 8 1/2" page at eight lines per inch. Characters are formed in a 16 by 16 dot matrix. Desktop units occupy 4.32 cubic feet and weigh 100 pounds. All models use 11-inch wide roll paper, 500 feet in length. 3200A printer/plotter: $11,400; 3250 printer: $10,500. **Versatec,** 2805 Bowers Avenue, Santa Clara, CA 95051.

Circle 209

COMPUTER SYSTEM

The Clerk 800 features a 16-bit single board processor with 64K memory (expandable to 256K), a 32Mbyte cartridge disk storage subsystem (expandable to 96M), a multi-tasking operating system, and Cobol applications software. Standard components of the Clerk 800 computer system also include: 24 line × 80 column video terminal; 200 cps bidirectional matrix printer; real-time multi-tasking operating system; Cobol run-time translator; Basic interpreter; an extended Fortran IV compiler and run-time library; and any one of the following applications software packages — general ledger, payroll, accounts receivable, accounts payable or inventory mamagement. **Retail Sciences,** Suite 254, 3384 Peachtree Rd. N.E. Atlanta, GA 30326.

Circle 188

4050 SERIES COMPUTERS

The 4052 and 4054 feature a Tektronix-designed processor and special memory architecture. Expanded graphics capabilities have also been added including a 19-inch DVST display on the 4054, which sets the 4054 apart from the 11-in. 4051 and 4052. With over 13 million addressable points, the 19-in. screen is said to make the 4054 the only desktop computer that can support 133 character lines of text allowing the user to preview full pages of computer printout at a glance. The three 4050 series products are 100% compatible in language, storage, and software and all 4050 series members support demand screen hard copy of graphics and/or alphanumerics. With a minimum of training, 4050 users can see graphic results instantly using Basic. The 4052 and 4054 have all the features of the 4051 including direct view storage tube for sharp, dense and stable graphics; internal magnetic tape drive with 300K bytes for data and program storage; and an IEEE std-488 (GPIB) interface. 4051: $5995; 4052: $9800; 4054; $16,500. **Tektronix, Inc.,** P.O. Box 500, Beaverton, Oregon 97077.

Circle 195

NEW PRODUCTS

BAND PRINTERS

The B-series band printers are available in 300, 600 and 900 lines per minute models. They are plug compatible to DEC's PDP-8 and 11 and DEC-20, Data General Nova and Eclipse (with

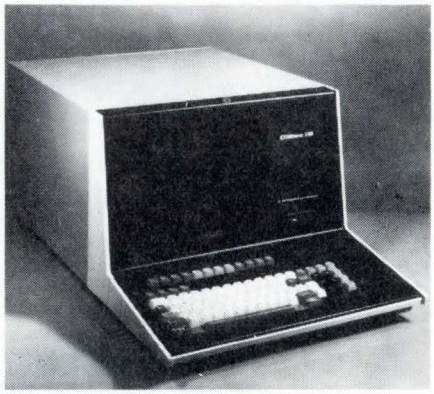
DMA attachment), Hewlett-Packard (including 3000 series), IBM Series/1, Interdata, RS-232C and other datacomm interfaces. Other features include ASCII print coding, 132 position line length, forms length selector switch, and 48 and 96 character sets. The 300 and 600 LPM models offer 15 character per inch density. $5,995 - $12,995. **Digital Associates Corp.,** 1039 E. Main St., Stamford, CT 06902. **Circle 214**

PRODUCTION DUPLICATOR

The UPP-2700 combines both EPROM testing and programming in one unit. It incorporates a circuit which evaluates all EPROMs both before and after programming. This circuit is designed to detect poorly erased or static damaged EPROMs which might otherwise pass a verify test. By pressing a single key, the 8048 processor tests and duplicates sixteen 2708's in less than 200 seconds. Complete system, including UPP-2700 duplicator, PM module, and power supply: $2450. **Oliver Advanced Engineering, Inc.,** 676 West Wilson Ave., Glendale, CA 91203. **Circle 212**

EXORterm 150 TERMINAL

The EXORterm 150 has been upgraded from the EXORterm 100 in that it has an improvedadds the cursor control, tabbing, page, line and character control keys. EXORterm 150 is an M6800-based system, using predominately LSI components of the M6800 family. It provides control of the display attributes, communication facility, terminal switch/indicator control, and keyboard inputs. The EXORterm 150 is housed in an enclosure, consisting of the following elements: a Motorola M3000 video monitor; a CRT controller board containing the necessary control electronics and firmware operating routines; a CRT configuration board providing the means to



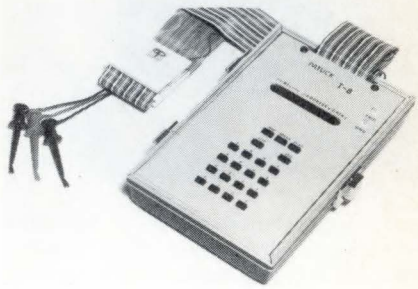
manually select basic operating criteria; a chassis/housing with power supply; a keyboard; and necessary resident executive firmware to control the display and communications interface. EXORterm 150, EXORcisor display console (110 V, 60 Hz option-part number M68--SXD10150): $2,490.00 (1-15). **Motorola Microsystems,** PO Box 20912, Phoenix, AZ 85036. **Circle 144**

9900 FAMILY DMA CONTROLLER

The TMS9911 generates memory control signals and sequential memory addresses for two separate DMA channels without the requirement of external devices. The TMS9911 can access memory autonomously with respect to the CPU providing input or output at a rate of 1 million 16-bit words per second. Additionally, multiple DMA's may be used to extend the number of DMA channels beyond two. Each of the two DMA channels has two 16-bit registers: a memory address register (MAR) and a last address register (LAR). The MAR contains the memory byte- or word-address which the next memory cycle by that channel will access. Initial access requires that the DMAC gain control of the system memory bus. When the DMAC has control of the bus, no other DMAC or the CPU may perform a memory operation until the DMAC completes its memory cycle. $15.40 (100). **Texas Instruments Inc.,** P.O. Box 1443, MS-6404 (Attn: TMS9911), Houston, TX 77001. **Circle 158**

TINY TOOL SIMPLIFIES MICROCOMPUTER DEBUGGING JOB

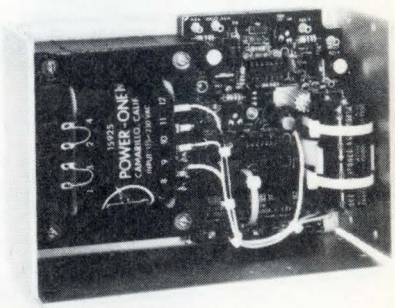
This low cost unit complements high priced microcomputer development systems. It can also be used for debugging where microcode is developed on a general purpose computer. A low-priced μC analyzer, called the Patuck model T-8,



was developed to make debugging a lot easier for design engineers. The tiny T-8, about the size of your hand, connects to the μC under test via a 40 pin chip clip. Optional microcomputer interfaces are available for the 8080, Z80, 2650, 6501, 6502, 6505, 8060, and 8085. The T-8 can single step the μP under test or let it free run to a T-8 selected error vector or trap address. Information is displayed and the problem analyzed on the T-8's 8-1/2 digit display. $695. Interface: $50. **Patuck Inc.** 5073 Russell Ave., Pennsauken, NJ 08109. **Circle 160**

FLOPPY-DISK POWER SUPPLY

The open frame CP-323 is designed to power two Mini-Floppy type floppy disk drives simultaneously. D.C. outputs provided are: +5V @ 2A with overvoltage protection set at 6.2V



±0.4V, and +12V @ 4A with overvoltage protection set at 15V ±1.0V. An inhibit function is also provided to allow the user to sequence the +12V output on and off using a low level TTL signal. Size is 7.00" × 4.87" × 2.75". $74.95 (1-9) **Power-One, Inc.**Power One Dr., Camarillo, CA 93010. **Circle 167**

ENHANCED 8048 FAMILY μCs

Centerpiece of the family is the proprietary INS8050 which contains 4K bytes of ROM and 256 bytes of RAM on the same chip as the CPU — twice the capacity of any similar single chip microcomputer now on the market, according to the manufacturer. The use of a powerful XMOS process is said to result in 8048 family devices which are 15 to 20% smaller in chip size, consume 20 to 25% less power in full operation and 12 to 35 times less power in the standby mode. Standby voltage is only 2.2, less than half that required for present NMOS 8048 devices. The family will initially include six single chip μCs, INS8048, which can operate as a stand-alone single chip system with programs stored in 1K byte of masked ROM and 64 bytes of RAM; INS8049, with 2K bytes of masked ROM and 128 bytes of RAM; INS8050, with 4k bytes of masked ROM, pin compatible with the 8048/8049; and 256 bytes of RAM on-chip; and INS8038, INS8030, ROMless versions of the INS8048, INS8049 and INS8050. **National Semiconductor**, 2900 Semiconductor Dr., Santa Clara, CA 95051. **Circle 244**

PAPER HANDLING DEVICES

The HyFeed cut sheet is an electronially controlled unit, easily installed on Diablo HyType and HyTerm printers and terminals which permits automatic insertion of up to 200 single sheets of 20-lb. paper. Using the HyFeed unit, printing from the extreme top of the page to the extreme bottom is possible. The unit can accept paper widths from 5-1/2 to 12′ and lenths from 3-3/4 to 14′. Mixed paper stocks of 18 to 24 lbs. can be used. Drive for the unit is provided by the printer's platen. HyFeed is installed via an interface option. **Diablo Systems Inc.**, 24500 Industrial Blvd., Haywood, CA 94545. **Circle 238**

GUEST PROCESSING WITH APL

An IBM 5100 or IBM 5110 computer may now sign on to the Sharp APL system as an intelligent terminal. This processing is established using the 51X0 serial I/O adapter feature, with the result that the power of APL is available at both ends of a phone line. The two APL workspaces — one on the 51X0 (guest processor) and one on the Sharp system (host processor) may be interfaced with either ASCII or EBCD. **I.P. Sharp Associates Ltd.**, 145 King St. W., Toronto, Ontario, Canada M5H 1J8. **Circle 258**

64 K BYTE μ SYSTEM

A two board μC system utilizing Digital Equipment Corp. LSI 11/2 cpu model KD11-HA with power fail/auto restart, 16-bit I/OP DMA port, real-time clock input and vector interrupt handling and Chrislin Industries' CI-1103 32K × 16 memory board is now available. The 32K × 16 dynamic RAM memory module hads an acces time of 300s from SYNC active. Cycle time is 525s. On board memory select is available in 2 K increments up to 128K words. Two boards, 8.5″ × 5″. $1250. **Chrislin Industries, Inc.**, 31312 Via Colinas #102, Westlake Village, CA. 91361. **Circle 187**

FOR AID—80F

The following software is available to augment FLP-80DOS (AID-80F operating software) and the capabilities of the AID-80F.

The Mostek Z80 macro assembler (MACRO-80) is an advanced upgrade from the FLP-80DOS assembler (ASM), and is fully upward compatible with all other Mostek Z80 Assemblers.

The Mostek 3870 Macro Assembler (MACRO-70) is an advanced upgrade from the FLP-80DOS Assembler for the 3870 microcomputer (FZCASM), and is fully upward compatible with all other Mostek 3870 Assemblers.

Mostek Basic is an extensive implementation of Microsoft BASIC for the Z80 microprocessor. Its features are comparable to those Basics found on minicomputers and large mainframes.

Mostek Fortran is comparable to FORTRAN compilers on large mainframes and minicomputers, It is unique in that it provides a μP FORTRAN and assembly language development package that generates relocatable modules.

Software Library - /Volume 1 is a library of 23 programs designed to run on FLP-80DOS. It is supplied on two diskettes. Source and object code supplied. MACR/80: $350.00; MACR/70: $650.00; Mostek BASIC: 325.00; Mostek Fortran: 600.00; Mostek Software Library: 250.00. **Mostek Corp.**, 1215 W. Crosby Rd., Carrollton, TX 75006. **Circle 224**

LSI — 11/VERSATIC CONTROLLER

The VIF 1200 for interfacing a Versatec electrostatic Printer plotter to an LSI—11, is contained on a dual width printed circuit board for LSI— 11/2 compatibility and plugs directly into the LSI—11 Q-BUS. The RT-11 software compatible controller comes with programmed device conttrol in both print and plot modes. In addition to diagnostic routines, Fortran callable print and plot routines are provided on a floppy disk. The VIF 1200 is supplied with a 20 foot cable for connection to the Versatec printer/plotter. **Image Automation, Inc.,**3350 Scott Blvd., Building 22, Santa Clara, CA 95051. **Circle 211**

CARD PUNCH CONTROLLER

The DP2029 controller allows punching of cads from any standard ASCII characters (plus 32 control codes in Monitor mode.) "Instant replay" allows viewing of either overstrike character separately. In either APL or ASCII mode, it will store (keyboard-entered or computer-loaded) up to 32 programmed functions — forms, answerbacks, control sequences — totalling more than 500 characters. $1,590.00 **Teleray Division,** Research, Inc., P.O. Box 24064, Minneapolis, MN 55425 **Circle 211**

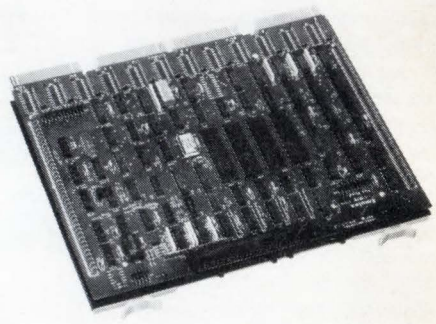
HIGH RESOLUTION COLOR GRAPHICS

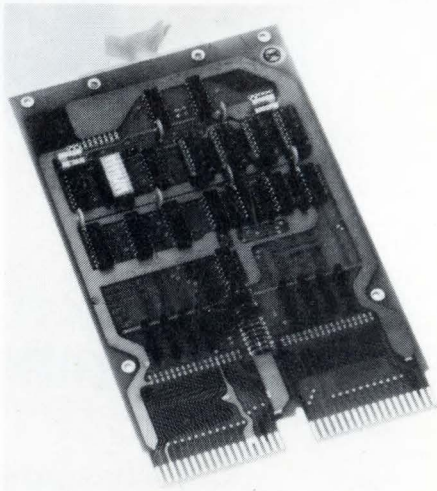
The RM-9400 display generator is available in six resolutions featuring a maximum of up to 1024 scan lines of 1280 elements and 128 bits-per-element — and for the first time offers users such high resolution in color, according to the manufacturer. Distributed processing concepts are executed in virtually every aspect of the display generation. Depending on the system's resolution, refresh frequency (frame rate) is either 50/60 Hz (repeat field) or 25/30 Hz (interlaced). The RM-9400 decodes and processes a high-level, binary formatted instruction set. The instructions, which are typically transmitted and received via a high-speed 16-bit parallel interface, can be executed immediately or stored as subpictures in user memory for deferred execution. Standard font for the RM-9400 contains 128 symbols defined within a 7 × 9 element dot matrix. Up to 15 additional fonts can be down-line loaded. Maximum font resolution is 16 × 20 elements; however, symbols can be magnified by pixel replication. **Ramtek Corp.**, 585 North Mary Ave., Sunnyvale, CA 94086. **Circle 201**

NEW PRODUCTS

LARGE DISK CONTROLLER FOR LSI 11

The μP based SC01 controller family includes three models which are fully compatible with DEC software and allow users to add as much as a half billion bytes of hard disk storage capacity to their LSI-11 systems. Said to be the first and only products of their kind, they are expected to open an entire new range of applications for the LSI-11. The basic SC01 family consists of three models, each designed to exactly emulate an existing model of large disk storage subsystem made by DEC. The SC01/A controller emulates the DEC RP11/RP02/RP03 subsystems; the SC01 emulates the RH11/RM02/RP04/RP05/RP06 subsystems; and the SC01/C emulates the RK611/RK06/RK07 subsystems. Each controller incorporates an automatic self-test capability plus extensive subsystem diagnostics in on-board firmware, and special operating functions can often be added to further enhance the system performance. $3,250 (50). **Emules,** 17785 D Sky Park Circle, Irvine, CA., 92714. **Circle 180**





FIXED CONSOLE EMULATOR

The Model 10047 Emuloader is a novel method to provide a fixed console emulator (ODT) as well as a bootstrap loader. The Emuloader improves the ease and utility of operation of several PDP-11 computers. The ODT for console emulation has not been available for many PDP-11 computers. The Emuloader provides for utilization of ODT functions by the computer from the console or most terminal devices. Additionally, when initializing through the ODT start address, a memory diagnostic is run on all installed memory. The Emuloader provides loaders for the DL11, PC11, RC11, RK06, RK11, RM02/03, RPOY/05/06, RP11, RS03/04, RX11, TC11, TM11 and TU16. Devices may be booted from the terminal via ODT or manually from the switch console by appropriate address. Since the Emuloader replaces the standard bus terminator, its advantages to the user may be realized without the loss of any backplane space in the computer. **Able Computer Technology, Inc.,** 1751 Langley Ave., P.O. Box 18162, Irvine, CA 92714. **Circle 192**

HIGH PERFORMANCE CASSETTE SYSTEM

Using standard Philips digital cassettes, the 374 reads and writes digital data in both diphase and ANSI formats. High performance, rugged transport design incorporates four separate DC motors to accomplish all tape loading and retracted by positive cam rotation. A operating system — CMTOS — is available with the Model 374. $3720. **Dicom Industries, Inc.** 715 N. Pastoria Ave., Sunnyvale, CA 94086. **Circle 221**

μP KEYBOARD LINE

The 6000 series product line is based on an economical mechanical switch, enabling the manufacturer to provide state-of-the-art keyboard features and performance at low cost. The keyboard line uses μP software capabilities to handle features such as 2-key and N-key rollover, tease protection, and repeat/auto repeat with a minimum of hardware. μP power eliminates the basic failure mode problems associated with mechanical switching and gives the series a price/performance advantage. The 6000 Series design is applicable to basic keyboard design formats as well as large custom versions with up to 128 keys. A number of standard and customized applications may be handled by means of changes to the modular software stored on the μP chip. Software modularity allows features to be added or modified without major redesign cost. **Maxi-Switch Co.,** 9697 E. River Rd., Minneapolis, MN 55433. **Circle 219**

COMPUTERS MAKE MONEY

Don Lancaster's 159-pg. book, "The Incredible Secret Money Machine," shows how to make your computer the core of your lifestyle — and how to make your computer expertise pay the bills. Lancaster shows how you could set up a μC consulting business, create software, write articles and books, design and manufacturer peripherals or kits. Chapters discuss getting started, keeping informed, tax dodges and investments. The book's best material (we felt) is in the two chapters on communications, ("Words" and "Images") and offers a 30 minute cram course in printed communication — whether magazine article, spec sheet, pamphlet or advertisement. "Words" gives you 16 pgs. chock-full of the essentials of good wiring, while "Images" offers an equally boiled-down intro to line art, camera work, layout and typography. $5.95. **Howad W. Sams & Co.,** 4300 West 62nd St., Indianapolis, IN 46268.

TRS-80 GRAPHICS

The 134-pg. paperback, "Introduction to TRS-80 Graphics" Don Inman, show how to create graphic displays writing Basic programs. It begins with fundamentals and works with line drawings and geometrics and finally moves into animation and more advanced operations. It compares plot versus print method and rectangular graphics, goes through bars, straight lines at odd angles, stationary and moving targets, bending straight lines and geometric figures. $8.95. **Dilithium Press,** Box 92, Forest Grove, OR 97116.

AOS PASCAL

Said to be the first commercially available Pascal compiler for Data General's newly developed Advanced Operating System. AOS is a multi-user multi-tasking operating system running on the Eclipse line of computers. The combination of Pascal's clear and structured approach to programming and an AOS timesharing system opens up many possibilities for on-line educational programming instruction and program development on a modest budget. AOS Pascal can also shorten program development time in production or research facilities with rapidly changing demands. Distribution of the Lancester/AOS Pascal Compiler includes both source code and binaries, on 9-track, 800 bpi magnetic tape, for $300. **Gamma Technology, Inc.,** 2452 Embarcadero Way, Palo Alto, CA 94303. **Circle 230**

HIGH RESOLUTION GRAPHICS GENERATOR

Using a 15", high resolution monitor, the GMDM-1000 generates a 1024 × 768 element display and is available with off-the-shelf interfaces for the DEC LSI-11, Zilog Z-80 and Intel 8086 processors. The GMDM-1000 displays the contents of a three quarter Mbit memory module. Through the use of the program controlled host I/O functions, the individual memory words can be written and read. In addition to the three boolean functions AND, OR & Exclusive OR, bit mode is supported so that individually addressable bits can be accessed. **Image Automation, Inc.,** 2250 Scott Blvd., Building 22, Santa Clara, CA 95051. **Circle 202**

DATA NETWORK/TERMINAL CONTROLLER

Called Vista/80, two products use multiple μP architecture and function either as an intelligent clustered CRT/Keyboard controller, or as a "hold and forward" data concentrator. A generalized modular design enables Vista/80 to accommodate changes in network functions, protocols and terminal devices, and to expand easily to handle network growth. The Vista/80 terminal controller will support up to 18 CRT/Keyboards or a combination of CRTs and printer devices. The Vista/80 data concentrator attaches to host computers through one or two 9600-baud lines, and supports up to eight 9600-baud circuits on the downline side. $6,000-$15,000. **Microform Data Systems, Inc.,** 830 Maude Ave., Mountain View, CA 94043. **Circle 288**

ERROR-CONTROL CODING

"Error-Control Coding and Applications" by Djimiti Wiggert is a 203 pg. handcover ($28.50) book that addresses the communications engineer's most vexing question: Is what you're sent what you get? And if not, how can you reliably detect and correct errors in data transmission with a maximum of speed and efficiency and a minimum of costly equipment and storage space? The latest and most useful error-control techniques are all presented in this one convenient volume. Parity check codes, cyclic convolutional codes, and BCH and R-S codes are detailed along with Threshold, Viterbi, and Sequential decoding schemes. Special chapters explicate coding to combat impulse noise in addition to applications and trade-off analyses. **Artech House, Inc.,** Dept. W-12, 610 Washington, Dedham, MA 02026.

CONTROL MODULES FOR STD-Z80 BUS

The first of a line of industial control modules compatile with the Mostek STD-Z80 bus is the MDX-SDI which is capable of controlling most stepper drive translators and motors. The MDX-SDI allows software control of pulse rate and ramping functions as well as position.

With the MDX-SDI, multiple stepper drives can be incorporated with less software overhead and greater throughput than with conventional techniques.Complete custom designed systems using STD-Z80 modules can be fabricated. **Industrial Dynamics Inc.,** 6929 West 130th St., Cleveland, OH 44130. **Circle 216**

ADVERTISER'S INDEX

SALES OFFICES

NEW ENGLAND and UP STATE NEW YORK: John A. Garland **(617) 934-6464** Box 314 SHS, Duxbury, MA 02332

MID-ATLANTIC and SOUTHEASTERN STATES: Ed Shaud **(215) 688-7233** P.O. Box 187, Radnor, PA 19087

MIDWEST and TEXAS: Hank Bean **(312) 475-7173** 2633 Hillside Lane, Evanston, IL 60201

WESTERN STATES: Al Puetz **(213) 478-3017** 924 Westwood Blvd. Suite 610, Los Angeles, CA 90024

JAPAN: Hiro H. Irie **(03) 311-1746** Intl. Business Corp., 11-8 Narita-Higashi 1-chome, Suginami-Ku, Tokyo 160

NEW PRODUCTS

DIGITAL IC TEST SYSTEM

The Inspector 100, a fully programmable digital IC test system, performs both functional and DC parametric tests from 14 - 24 pins which operate from 4.5 to 5.5V. The Inspector 100 is controlled by a complete 8085 μC system. It has 32K bytes of memory, dual floppy disks, a built-in 9" CRT and a keyboard. A printer option is available. The Inspector 100 is controlled by the TBASIC test language to include a set of tester control functions. TBASIC features test statement syntax, full BASIC functions, floating point arithmetic, automatic pin by pin failure analysis, failure categories, and data logging on console or printer. TBASIC programs are loaded and stored on one of the systems disks, with up to 64 programs per disk. Inspector 100: $8900; printer option: $2800. **Pragmatic Designs, Inc.,** 711 Stierlin Rd., Mountain View, CA 94043. **Circle 256**

PROGRAMMABLE SWITCH

A programmable display switch that can be set manualy with input to the CPU can also be programmed by the CPU to a full hexidecimal range. Available in three manual ranges, decimal, hexidecimal and octal, all modes are jumper selectable. Up to sixteen modules can be used with I/O multiplexing and TTL compatibility. The deisgn uses 3/8" characters. Interconnect is by standard connectors and flat ribbon cable asemblies. The DTL assembled programmable switch is aid to cost less than a thumbwheel switch and related components which it replaces. **Diagnostic Testing Laboratory, Inc.,** 7150 Hart St., Mentor, OH 44060. **Circle 290**

IC INTERFACE TO IEEE BUS

The HEF4738V LSI circuit is for use with bus-drivers, level converters and multiplexers, to connect electronic programmable for non-programmable equipment to an IEC/IEEE bus. The HEF473V features complete source and acceptor handshake, a basic talker with serial poll and talk-only mode, and a basic listener with listen-only mode. The device also includes complete service request and remote local, as well as remote parallel poll configuration. It has complete device clear and trigger with some controller facilities on the LSI chip. Supply voltage rating for the circuit is -0.5 to +18V, with a recommended operating voltage of 4.5 to 12.5 V. The DC current into any input or output is a maximum of 10 ma. $26.25 (25-99). **Signetics,** P.O. Box 9052, 811 E. Arques Ave., Sunnyvale, CA 94086. **Circle 291**

ECONOMICAL MEMORY TESTER BY RELIABILITY

A series of functional memory testers, capable of handling static and dynamic devices with capacities up to 16K, administer pass-fail tests to all locations of the device under test in less than 0.2 second. Power source for the tester is a rechargeable nickle cadmium battery. $98.50. **Reliability, Inc.,** P.O. Box 37409, Houston, TX 77036. **Circle 231.**

EXORCISER BUS CRT CONTROLLERS

The EXO-2480 Motorola Exorciser bus compatible alphanumeric CRT controller provides 96 ASCII characters with descenders plus 32 graphic symbols in one 24 × 80 page or two 24 × 40 pages. Normal or inverse video, with or without blink synchronized internally or externally (TV camera or VTR) are available on the EXO-2480. The EXO-512 may be used to provide a high resolution graphics, 256 vertical × 512 horizontal display or two independent 256 × 256 images. Both boards may act as master or slaves in an alphanumerics/graphics application. The memory as well as the display on both boards is automatically refreshed. Addressing for the graphics board is accomplished in an X-Y matrix and the RAM is located in the I/0 area. EXO-2480: $495; EXO-512: $695. **Matrox Electronic Systems Ltd.,** 2795 Bates Rd., Montreal, Que., Canada H3S 1B5. **Circle 203**

EXORDISK III SYSTEM

The EXORdisk III (M68SFD1102) consists of two double-sided/single-density drives in a compact tabletop cabinet, a controller board and an interconnecting cable addembly from the controller to the disk drive unit. Circuitry is included for head unload timeout and a write protect feature for protection of master disk programs. The drive enclosures contain power supplies for all voltage requirements. The EXORdisk III expansion unit consist of 2 additional drives in an enclosure, plus the cable required to connect the drives to the system. The disk operating system— MDOS 3.0 — supplied for use with the EXORciser products, is supplied on one disk. EXORdisk III features includes: 512 bytes/disk; 1543 tracks/disk; 26 sectors/track; and 128 bytes/sector. M68SFD1102: $4800; M68SFDU1102E: $4200. **Motorola Microsystems,** P.O. Box 20912, Phoenix, AZ 85036. **Circle 226**

80 × 24 VIDEO BOARD

An 80 × 24 video board with hardware scrolling, x-y addressable cursor and multiple character generators for the SS 50 bus allows user-defined programmable character sets. It includes a TMS 2716 EPROM that contains a full 128 upper and lower case ASCII character set with true descenders; plus 2K of RAM for user-defined programmable character sets. The user can choose and intermix 384 different character generators and display up to 256 at one time, normally or inversely, and at ful or half intensity, at any location on the screen. Contiguous 8 x 10 character cells permit solid lines and connecting patterns with user definable graphic elements. **Gimix Inc.,** 1337 W. 37th Place. Chicago, IL 60609. **Circle 246**

Z80/8080 CONVERSION PACKAGE

Engineers developing programs for either the 8080/8085 or Z-80 processors or both, will no longer be handicapped by the different mnemonic used by the Intel of Zilog source code conventions. With the "ZIP" (Z80/8080 source program conversion) package, the user may write programs in either the Intel to Zilog source code convention, which can later be converted to a designated source statement form. The ZIP package contains two programs that are written in MACRO-11. The I80Z80 program converts the source program from the Intel 8080 mnemonic to the Zilog Z-80 mnemonic and the converts the source code from Zilog Z-80 mnemonic to the INTEL mnemonic. $250. each or a combined puirchase of $350. **Systems & Software, Inc.** 2801 Finley Rd., Suite 101, Downers Grove, IL 60515. **Circle 225**

LETTERS

Continued from p. 8

Dear Editor:

No exams? What else is new? This is typical of the "don't do as I do, but do as I say" mentality held by most leadership in this country today. Don't get excited, it's not going to change.

R.T.F.
Sacto, CA

Dear Editor:

Degrees from open universities are as much value as Monopoly money! Technicians are not engineers; an engineer is not only a problem solver, but also a problem finder, through rigorous training in a diverse assortment of fields, including the arts and humanities. All the lab bench experience in the world cannot equal that.

L.S.
Skokie, IL

Dear Editor:

Open universities? This revolting development is nothing new. There have always been diploma mills. The disgraceful part is that some people are now accepting them as legitimate — a sad lack of standards.

Prof. L.E.B.
Toledo, OH

Are Discretes Dead?

Dear Editor:

I read with interest your January Viewpoint, "Who Says Discretes Are Dead?" by John Welty, Vice President of Motorola and would like to add some observations regarding the optimistic outlook for discrete components. Mr. Welty generalizes, lumping all the discretes together — a broad generalization that does not permit making as accurate a forecast as he would find necessary to re-orient Motorola's marketing projections. Discretes fall into several categories (such as capacitors, resistors, diodes, transistors, thyristors, optoisolators and so on). Furthermore, these categories, in turn, are subdivided. Certainly, power and small signal transistors will fare differently; and sales of board-mountable resistor networks housed in DIPs may fare better than standard resistors. Obviously, some of these categories and subcategories will fare well and other won't.

Another fact not addressed was the effect of single-chip microcomputers. Although the increased usage of microcomputers will increase the demand for discrete components, micros are using less external discrete devices, and component costs have dropped drasticallly and will keep dropping. This will affect the demand for certain discretes more than others. Another factor affecting demand will be future application categories, which will be in different ratios in the 1980s than we see today. A given micro used in an industral application may require more discretes then if used in a consumer product.

What this means for designers is altogether a different matter, and the increasing demand for discretes should not lull older engineers into complacency. Certainly, the near-term growth in most discrete sales is not going to be reflected by any significant upsurge in demand for engineers with these older design skills.

H.V. Belsan
Palo Alto, CA

NEW PRODUCTS

GENERAL LEDGER IN BASIC

"General Ledger", the third book in Osborn & Associates' series of Basic business program books by Lon Poole and Mary Borchers, includes program listings with remarks, descriptions, discussion of the principles behind each program, file layouts and a complete user's manual with step-by-step instructions, flow charts, and sample reports and CRT displays. The program listings are in Wang Labs extended Basic. (The book describes how these listings can be made compatible with other versions of Basic.) It has been written to share common files with the two otehr books inthe Basic program series ("Payroll with Cost Accounting " and "Accounts Payable and Accounts Receivable"), ISBN 0-931988-20-9, 160 pp., 8-1/2 × 11" paperback. $15. **Osborne & Associates, Inc.,** 630 Bancroft Way, Berkeley, Calif. 94710.

LSI-11/23, PDP-11/23 μCs

Said to be the world's most powerful μC, the LSI-11/23 has the functionality and software compatibility of a midrange mincomputer, yet consists of only two 5.2 × 8.9-inch boards and backplane. A rack-mountable, package version, the PDP-11/23, is also available. This is the first μC offering with a full floating-point hardware implementation, claims the manufacturer. The LSI-11/23 features 256 K bytes of memory capacity, four times greater than the low-end LSI-11/2. It uses the full instruction set of the PDP-11/34 minicomputer, and software-supported memory segmentation and protection features of the RSX-11M and -11S multitasking, multiuser operating systems. The LSI-11/23 has the same size circuit boards as the LSI-11/2. Besides accommodating RSX-11M and -11S software, the LSI-11/23 and PDP-11/23 run all software developed for the LSI-11 family without modification. This includes the RT-11 operating system and high-level languages including BASIC, FORTRAN IV, and FOCAL. Depending upon configuration, the LSI-11/23 is said to be from 2 to 5 times faster than previous LSI-11 family members. LSI-11/23: $1,758 (100); PDP-11/23: $4,500 (100), $6,800 (1). **Digital Equipment Corp.,** Maynard, MA **Circle 233**

ZILOG'S 1ST DATA BOOK

The "Zilog Data Book" is the first compilation of detailed specifications for Zilog's components, boards and development systems. The 132-pg. book is aimed at design enginers who will use Zilog products in constructing their own μC systems. It includes sections on the Z-80 family of MOS LSI μC components, Zilog memory components, the MCB series of μC board products and the ZDS-1 series of MDSs. $5. **Zilog's Literature Dept.,** 10340 Bubb Rd., Cupertino, CA 95014. (408) 446-4666. **Circle 232**

VIDEO TIMER/CONTROLLER CHIP

A silicon-gate, N-channel MOS device, the TMS9927, offered in a 40-pin DIP, generates video display timing signals for a standard and non-standard CRT monitors that incorporate both interlaced and non-interlaced formats. The TMS9927 may be used with either 8 of 16 bit processors as a memory-mapped input/output device. Five sections comprise the new video timer/controller: CPU interface, cursor control, horizontal control, vertical control and self load. Plastic: $22.50 (100); ceramic: $27 (100). **Texas Instruments Inc.,** Inquiry Answering Service, P.O. Box 1443 M/S 6404, (Attn: TMS9927), Houston, TX 77001. **Circle 220**

APPLESOFT II BASIC MANUAL

An unusually complete programming reference manual, for the Applesoft II language, fully describes the extended programming capabilities which Applesoft II Floating-Point Basic offer. Applesoft II is an expanded version of Basic. Its 9-digit arithmetic and large function library make it better suited for business and scientific applications than Integer Basic. The Applesoft II reference manual assumes that the reader has a working knowledge of Basic and only wants to learn the additional features offered by Applesoft II; it is not intended as a text on Basic. A handy "Quick Reference Guide" to all variables, operators and commands in Applesoft is located in the front of the manual. $6.95. **Apple Computer, Inc.,** 10260 Bandley Dr., Cupertino, CA 95014. **Circle 215**

PROM PROGRAMMING SYSTEM

The Smarty is a Universal Prom Programming system with features not found in other programming systems. A new concept, Permanently Connected Slaves, eliminates the need for changing personality modules and pinout adapters. (No pinout adapters required: no configuration adapters required.) Single Unit, Family, FPLA and Sweet Sixteen slaves are available for programming all types of Proms. The Smarty SM-100 Master unit includes a built-in 2708/04 Programmer. The uniqued Family EPROM slave programs all the popular development type EPROMS including 2716(I), 2732(I), 2758(I), TMS 2716(TI), TMS 2516(TI) and TMS 2532(TI). The Smarty has a built in Prom simulator and editor. This feature lets the user interactively debug his software without having to burn in a Prom with each iteration of a change. The simulator is available in 8K, 16K, 32K and 64K bit sizes. The larger versions are user configured as 8 bit, 16 bit or 32 bit words. The Smarty software includes 12 different Editing, Loading and Listing commands as well as Verifying, Comparing and Programming commands for each Prom. With the optional Micro Cassette the commands include several read, write and compare functions. Price of the Smarty including the built-in 2708/04 Programmer, Prom Simulator and all features listed is $1,695; Unit and Family Slaves, $275 to $450 each. **Sunrise Electronics,** 307 S. Vermont Ave., Unit H, Glendora, CA 91740 **Circle 218**

TAPE CONTROLLER FOR PDP-11

A μP-based tape controller, the Model TC11, is designed to provide complete compatibility with DEC TU10/TM11 tape subsystems for PDP-11 users. The TC-11 may be used with any industry standard reel-to-reel magnetic tape drives— including NRZ, PE and Dual Density — up to 125 ips. It can be installed in just one (NRZ) or two (PE and Dual Density) existing SPC slots of the user's backplane or system unit. The TC11 executes all DEC PDP-11 system and diagnostic software without modification. $2,250 (NRZ) and $2,700 (PE and Dual Density) (50 units). **Emulex Corp.,** 17785 D Sky Park Circle, Irvine, CA 92714. **Circle 227**

VIEWPOINT

Robert Howard, *President*
Centronics Data Computer Corp.

Vertical Integration: Road to Success or Failure?

A manufacturer who does not look down the long list of major items his company purchases from outside vendors and ask, "Can't we make some of these things cheaper ourselves?" isn't watching his business the way he should. After all, that's what business and competition is all about: making something better and less expensively.

But there are as many dangers in the build decision as in buying; and for a high technology firm to think it can do anything and everything is simplistic. The firm that doesn't carefully control its instinct to integrate may batter the bottom line. Such a hastily-made decision inevitably ends up as a failure that demotivates people, negtively impacts the corporation's principal finished product, causes lost marketing opportunities and reduces overall competitiveness. Failure can be avoided if certain guidelines are followed. First, beware of corporate emotionalism. Too many companies allow their pride and company patriotism to lure them into an effort which enhances their self-esteem — not their self-preservation. Other, less worthy motives to integrate include empire building and corporate politics.

Usually, though, genuine attempts are made to test the economic practicality of manufacturing a product or providing a service previously supplied by a vendor. The task often appears simple, and management reasons that even if the economic projections aren't 100% accurate, their engineers indicated a safety margin for error. A quick and sweeping evaluation of integration feasibility usually turns up encouraging go-ahead signals such as underutilized manufacturing facilities, manpower inefficiencies, visions of future growth possibilities, excellent anticipated volumes and assurances that major manufacturing investments will be minimal. Long term prospects look good.

But a closer look (often made in hindsight) shows hidden costs that even the most experienced firms often miss. It is extremely difficult under any circumstances for anyone to justify a short-term vertical integration effort. On the other hand, it is very easy to be trapped into believing that a long-term commitment is being made when in reality, less than full consideration is being given to all that a long-term effort will require. Therefore, the planned long-term project dies an untimely, economically unjustifiable death. Why does the long-term approach quickly become a short-lived endeavor? Because it's simple to copy today's technology but difficult to copy tomorrow's, which is only now being developed as a result of massive research and development costs only the most resourceful companies can afford. As a result, the firm that hastily integrates (but must take 18 months to two years to get to production) often finds that in a very short time its integrated product isn't competitive any longer. For example, computer manufacturers integrating to printers can soon lose system business or find that third party or foreign peripherals are being attached to their system. That's why so many printer integrators have COME and GONE over the years — losers in the never-ending race for the edge in R&D, manufacturing and technical know-how.

This raises another question: just how sophisticated is the product to be vertically integrated? It appears that a product or commodity's sophistication — be it a printer or any other highly technological device — is directly related to how difficult the vertical integration effort will be. If the integrated product is a bolt or screw or in a similar area where technology has reached a plateau, that's one thing; if, on the other hand, it involves constant custom engineering and state-of-the-art upgrading, vertical integration will be vastly more expensive and time consuming. In vertical long or short term integration, there is a price to pay for lost opportunities resulting from transfering product experts from their field to work on integration. There are the costs of either obtaining a specialized marketing and sales group or retraining and re-educating an existing group. And, only continuous, aggressive and heavy investments in research and development will help guarantee the competitiveness of the integrated part, device or sevice. Without this, a company's bottom line can be furtively eroded. All of this raises one last, generally ignored, consideration: disintegration costs. Failure takes its toll both in terms of dollars and time invested as well as the impact it can have on people and their perception of a company's strength. After all, it is much easier to "fire" a supplier.

Despite successful integration efforts, it's more common to see a combination of some successes and failures. For example, of the OEM's who decided in the last few years in favor of highly technological printer integration over the purchase of printers from dedicated manufacturers, many abandoned the effort. We are now completing the successful vertical integration of mechanisms — but, only after an outlay for capital equipment over the last two years of over $1 million for costs associated with specialized machinery and associated staff. Still, mechanism making involves manufacturing stamped or machined parts and not highly technical electronic systems or devices. True, the techniques of carriage casting and sheet metal fabrication take time to master and involve a large initial investment for machnery, staffing, tooling and set up. But very little else in the way of technology will be required in coming years. But in other areas, we find it more practical to purchase parts from others or to combine our manufacturing abilities with our suppliers to assure greater security of source.

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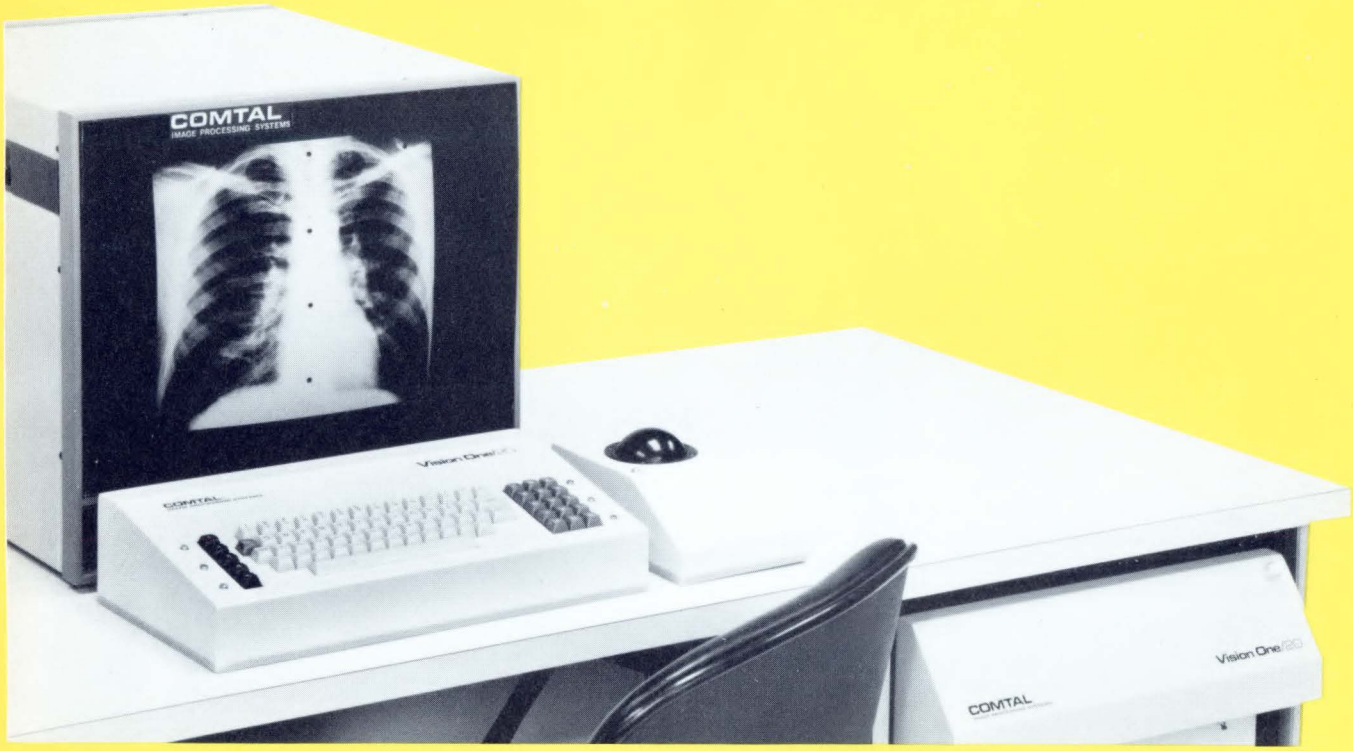

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