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REVOLT WITHIN THE RACK

Design isn't what it used to be. Today's designer has available a ready-made solution to major problems—a minicomputer. Like the miniskirt, the small general-purpose computer presents the same basic commodity in a more appealing way.

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Yesterday, the engineer had to design a one-of-a-kind circuit; today he has a widening choice of programmable computers that can be interfaced easily with his system. A staggering number of versatile, inexpensive computers are being manufactured by established companies and by new firms introducing their first marketing product. This sudden outburst of minicomputers stems from the growing acceptance of the general-purpose computer as an element of all digital systems coupled with a dramatic decrease in IC production cost.

Minicomputers can be applied to many fields—including the testing of everything from IC's to missiles, process control, biomedical electronics, data acquisition and data reduction. The advantages of using a computer to satisfy digital design requirements are many. Examples: development is accelerated because both hardware and software are evolved concurrently; for the price, computing capability cannot be duplicated; growth potential of the system and the software make the computer ideal for development, and the useful life of the computer-based system is longer than its hard-wire counterpart.

What Is a Minicomputer?

Principal attributes of today's computers, aimed at the OEM system designer, are summarized in the **Table.** This survey characterizes a **typical** computer as follows:

- Costs less than $35,000
- Easily programmed
- Very reliable
- Modest facility requirements
- Good interrupt structure
- Easily interfaced

Survey data were compiled from a number of sources, with the majority of the material obtained from literature or by direct conversation with marketing representatives. Quoted prices are for basic machines and do not include taxes or quantity discounts. Computer characteristics are defined on page 53. Some aspects of this computer class are not stated explicitly. For instance:

- All machines have an input/output capability from the accumulator register.
- None requires special air-handling equipment.
- 60-Hz power is standard with exceptions noted.
- A loader, assembler, utility and CPU diagnostic programs are provided for all machines with exceptions noted.

The New Breed

The proliferation of small computers attests to the potential of the marketplace. Basic machines start with a storage capacity of 4069 words or less, the barest logical essentials and a low price tag. Their modular construction permits the user to purchase only the com-

puting power he needs. The teletypewriter is the standard programmer/operator interface. Multiply/divide and floating-point arithmetic usually is optional. Typical machines are single address, have parallel arithmetic and represent numbers in two's complement.

Bit length of the computer word is a characteristic with important ramifications. Some significant considerations are:

- Memory cost and compute capability are directly proportional to word length.
- Data communication usually occurs in 8-bit bytes.
- Common physical measurements (from analog transducers) are in the 10- to 14-bit range.

Generally, processors with shorter words require a more involved addressing scheme and a heavier dependence on double-word instructions. This results in longer programs and increased running times.

Storage function for these computers is accomplished by a magnetic-core memory with a read-write cycle of 1 to 2 μs. Memories produced today are extremely reliable and account for about 50 percent of the system cost. Error detection by means of a parity bit per word is optional or not available.

The number of instructions available to the programmer also is related to word length. The two principle components of an instruction word are the instruction field and the address field. Instructions that do not address the memory use the address field for specification of shift counts, constants and other variations of a generic instruction. In some computers, a fast read-only memory (ROM) decodes both the generics and subcommand steps – a technique called microprogramming. Often microprogramming is used to generate special instructions that might otherwise require a software subroutine. In hardware-software morphology, this technique is called "firmware".

There is a trend toward more general registers in the central processor unit (CPU) – a characteristic adopted from the large-machine architecture. In the past, a double-length arithmetic register and a separate index register were the standard complements of the small computer. Today, programmable registers are more numerous and more imaginatively used. For example, the MICRO 810 has 15 registers that can serve for addressing, arithmetic or masking purposes and the DATA 520I has two independent sets of registers that simplify program environment changes.

The following addressing modes are of particular interest to the small-computer user.

DIRECT ADDRESSING – memory area or "page" is accessible by an absolute specification within a single instruction.

INDIRECT ADDRESSING – instruction refers to an address contained in an address.

INDEXING – one or more registers arithmetically combined with direct address in the instruction word.

RELATIVE ADDRESS – the programmer arithmetically combines a value in the instruction word with the program counter (counter that controls program sequence and specifies the address of the current instruction).

Relative addressing has been a feature of assembler language for years, but the generated code of the assemblers might contain indirect references. With this method of addressing, the programer has access to any memory location within K-locations of the current instruction.

One other technique worth mentioning uses a special register called a paging register to append high-order bits to the program counter.

Data Manipulation

Usually the small computer is dedicated to operations where transferring data in and out of core is the principal activity. All computers share the following characteristics:

- Input and output are functionally identical and use the same hardware.
- Lower bound on transfer rate is determined by word-at-a-time transfer through a CPU register.
- Higher data rates are achieved by block transfer of memory words independent of CPU control.
- Upper-bound transfer rate approaches memory rate.

Various hardware configurations have been developed to facilitate block transfer of data. Each data path is called a channel. Special registers for block addressing and limit checking accelerate channel operation. Maximum data rate is equal to the rate of reading or writing in memory. In more sophisticated systems, this function is independent of the CPU; thus, the processor can carry out computations with its registers and other memory modules in certain, usually optional, configurations.

Interrupts signal the occurrence of a change in both internal and external environments. For example, an external interrupt may signal the completion of a data-block transfer or the occurrence of a random event. Internal interrupts may flag a power failure or illegal instruction. Real-time tasks require extensive use of the machine's interrupt structure. The effect of an interrupt is to transfer operation from the current program to the interpreting routine. Processors with multiple levels of interrupt have a significant average-speed advantage over those machines with a single level coupled with a software decoding process.

Comparison, Selection and Use

It is the manufacturer's intent to supply a generalized compute (and storage) function at the lowest pos-

sible price. For this reason vast software libraries can be costly. Language compilers, operating systems, even relocatable assemblers usually are not required for the small machine dedicated to a single function.

Comparing similar machines is difficult. Trade-off of capability and marketing factors is supported by a thorough knowledge of the problem at hand. Many available speed/design/price combinations dictate that a successful selection can best be made by actually programming benchmark problems or, better yet, the kernel routines of actual application. Caution must be used when extrapolating to larger configurations because the ideal basic machine for a specific problem may be clumsy and expensive when expanded to meet larger requirements.

Peripheral equipment was not considered in this survey. With option, however, most machines have interfacing capabilities for peripheral equipment—especially the large-computer manufacturers. Peripherals in relation to the computing equipment are both expensive and unreliable.

Customer service is the marketing hallmark for the giants of industry but is the most unpredictable quantity in the small-machine world. Vendors clash with other vendors for 5 percent of the $6-billion annual computer market. The economics of minicomputers argue that one sells in quantity and does little customer hand-holding. Consequently, field-engineering support weakens for both new and established firms.

The age of the minicomputer is upon us. For good or ill, automata now are priced within reach of most engineering tasks. The effects will shake up many technical areas; historically sound methods that have become comfortable ruts for a lot of designers are being either replaced or revised. Designers, engineers and technical managers who are insensitive to change will be profoundly disturbed.

Databank

Mr. Linton and Mr. Ollivier recommend these references:

1. "A Pocket Guide to Hewlett-Packard Computers", Publication No. 5950-8313, Hewlett-Packard, Palo Alto, Calif.
2. "Varian Data 620/i Computer Manual", Bulletin No. 605-A. Varian Data Machines, Irvine, Calif.
3. "Specifications for the DRC Model 44 General Purpose Processor", Bulletin H-16, Dynamics Research Corp., Stoneham, Mass.
4. "DC-6024, General Purpose Computer Reference Manual", Reference Manual RM-60-2-169, Datacraft Corp., Fort Lauderdale, Fla.

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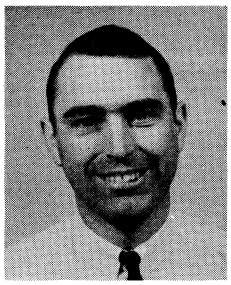

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LINE ITEM DEFINITIONS

Category	Characteristic	Definition
CLASS	Word size	Length of CPU word in bits. (Memory word length may be extended to include parity, protect or use bits.)
	Cycle time	Memory access time in microseconds.
	Price	Cost in thousands of dollars for the basic machine.
MEMORY	Basic size	Number of words in basic machine.
	Maximum size	Maximum memory size in words.
	Parity/protect	(Yes) if parity check made on each memory reference/(Yes) if a protect or use bit exists in each memory word. (Area) indicates a block of memory may be reserved for privileged use. CPU checks effective addresses.
INSTRUCTION SET	Number	Unique instructions in assembly language. Only generic commands are counted. Microprogrammed I/O and register functions counted once.
	Multiply	Hardware multiply time in microseconds. (SW) indicates no multiply hardware available.
	Indirect address	(K) K-levels of indirect addressing are permitted.
	Remarks	Instructions of unusual power are noted. Use of ROM memory to decide instructions noted. Ability to redefine or extend instruction set reported.
REGISTERS	General	Programmable arithmetic and index registers reported. A, X, P indicate Accumulator, Index and Program Counter. No A, X or P indicates general use as accumulator or index. Register length is in parentheses.
	Special	Programmable link, overflow, masking and paging registers noted, length in parentheses.
	Total bits	Number of bits in all programmable registers (machine status).
I/O	Word rate	Maximum word-transfer rates for basic and largest single processor configurations in MHz.
	Channel types	This item refers to buffered channels. All computers considered have basic I/O to/from the Accumulator register. Three types of channels for block data transfer are defined: SEL: Selector channel, one device active for block transfer. MPX: Multiplex channel, several devices may be active at one time, device scanner cycles for each word transferred. DMA: Direct access to memory without cycle stealing from CPU for addressing or block limit check.
	Number of channels	Number of buffered (DMA, SEL, MPX) channels in basic and maximum machines.
	Cycles stolen/word	Cycles lost to the CPU for each word transferred by a buffered channel. Range shows several types of channels.
	Sense lines	Method by which binary signals may be most easily interfaced. (DL) means channel data lines used.
	RT clock	An interrupt generating timer. Note frequency.
	Price includes	Peripherals included in the price of the basic machine.
	Interfacing	Note interface characteristics: method of connection, cable constraints, logic levels, etc. Number of devices that may be addressed in basic and maximum configurations shown.
INTERRUPTS	Number	Number of external interrupts in basic and maximum machine.
	Enable/disable	Method of arming/disarming interrupts: group (G), singly (S) or masked selection. If by group, note group size.
	Priority	Note levels of priority, basic to maximum. (Priority is method of ordering simultaneous interrupts.)
	Minimum service	Least time in microseconds from interrupt to first instruction in service routine.
	Power failure/restart	Power-failure interrupt and automatic startup capability.
	Remarks	Unusual features of scanning, status store on interrupt, internal interrupts, etc.
PRODUCTION	1st delivery	Month/Year of delivery of first unit
	Number sold	Approximate number of units in field
	Physical size	Height x Width x Length in inches. 19-in rack-installation size used when possible.
	Power	Watts of 125V 60-Hz single-phase power, unless otherwise noted.
OTHER FEATURES	Software	Significant features in addition to assembler and utility package are noted. Memory size noted if compiler requires more than basic size.
	Remarks	Features of the machine not noted elsewhere. Reliability, construction, relative addressing, sense switches, etc.

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PARAMETER \ COMPUTER		ADVANCE 6135	BIT 480	CAI 208	CAI 216	CAI 808	CAI 816	CDC 1700	VARIAN 5201	VARIAN 620i	DATA MATE 16	DC 6024/3
	Manufacturer	EMR	Business Info. Tech.	Computer Automation				CDC	Varian Data Machines		Datamate	Datacraft
	Location	Minneapolis Minn.	Natick, Mass.	Newport Beach, Calif.				Minneapolis Minn.	Irvine, Calif.		Big Spring, Tex.	Fort Lauderdale, Fla.
CLASS	Word size	16	8	8	16	8	16	16	8	16, 18*	16	24
	Cycle time	0.5	3.0	2.67	2.6	8.0	8.0	1.1	1.5	1.8	1.0	1.2
	Price	31.5	9	5.9	12.9	4.9	9.9	37.5	7.5	13.9	14.9	29.8
MEMORY	Basic size	8k	1kB	4k	4k	4k	4k	4k	4kB	4k	4k	8k
	Maximum size	32k	65kB	16k	32k	16k	32k	32k	32kB	32k	32k	32k
	Parity/protect	Yes/yes	Yes/no	No/yes	No/yes	No/yes	No/yes	Yes/yes	*/no	No/area	*/no	Yes/*
INSTRUCTION SET	Number	100	58	76	176	73	176	72	59	107	104	563
	Multiply	4.5-8.3	SW	1 ms-SW	42 μs	6 ms-SW	164 μs-SW	7.0	-	18*	7	9.6
	Indirect address											
	Remarks	DP arithmetic double indexing	• Variable word length • Decimal mult/div*	Add 8μ	5.3 μs	Add 24μ	Add-16μ Relative addressing	• 14 inst. groups	• Direct address to 4k	• Rel. address +512 • Micro-prog.*	• DP arith. • Byte processing • Mult. & div.	FP *
REGISTERS	General	2A, 3X	1A	1A	1A, 1X	1A	1A, 1X	2A, 2X	4A(16), 2X(16)	1, 1A, 1X	1A, 1X	5
	Special	–	1	0	0	0	0	–	2(6)	–	–	3 may be used as X
	Total bits	80	9	8	32	8	32	64	102	48, 54	32	120
I/O	Word rate	1.1	–	67	0.187	0.16	0.125	0.09-0.9	0.67	0.18-0.2	1.0	0.85
	Channel types	All	DMA, SEL	Auto I/O	DMA*,MPX	Auto I/O	DMA*, MPX	DMA*	SEL, DMA*	SEL	MPX, DMA	DMA*, daisy chain
	Number of channels	0-6	1-4	1-256	1-256	1-256	1-256	2	0-1	0-1	1-64	1-8
	Cycles stolen/word	0-4	1	4 Auto I/O	4	4 Auto I/O	4	1	1	2	1	1
	Sense lines	* groups of 16	8 DL	8 DL	16 DL	8 DL	16 DL	16 DL	8 DL	* groups of 8	16 DL	24 DL
	RT clock	*	*	60 Hz	*	60 Hz	*	Yes	–	*	Types*	Interval timer*
	Price includes	ASR-33	ASR-33	Console	Console	Console	Console	Console	Console	ASR-33	Console	ASR-33
	Interfacing	• 8-* devices • 30' & 1000' drivers • Two memory buses	• Up to 64 devices • Analog & digital peripherals	• Directly to DTL-IC's • Party line I/O bus • 3 priority interrupts	• Directly to DTL-IC's • 20-I/O instructions • 4-I/O slots main frame	• Directly to DTL-IC's • Party line I/O bus • 3 priority interrupts	• Directly to DTL-IC's • 20-I/O instructions • 4-I/O slots main frame	• Transmission of 8 or 16 bits	• Party line to 30' • Duplex lines • "A" to 16-bit channel*	• 1-64 devices • Duplex lines • PL to 20' • NPN & PNP I/O levels	• Up to 64 indiv. buffered devices/controllers	• TTL drivers • 8 buffered IOC's • 6-I/O insts. • 4 automatic block* controllers
INTERRUPTS	Number (min/max)	2-131	1-*	3-64	3-4000	3-64	3-4000	2-16	11-13	0-64	8-64	4-24
	Enable/disable	S	S	G-S	G-S	G-S	G-S	S	G-S	G-S	S	G-S
	Priority levels	2-131	1-*	64	1-126	64	1-126	2	4	0-64	8-64	4
	Minimum service	6.0	–	3.0	3.0	3.0	3.0	2.2	1.5	3.6	3.0	2.4
	Power failure/restart	*/yes	Yes/yes	*/*	*/*	*/*	*/*	Yes/yes	*/*	*/*	Yes/yes	*/*
	Remarks	Registers saved in core	–	Expandable in groups of 8	Expandable in groups of 8	Expandable in groups of 8	Expandable in groups of 8	Registers saved in core	Operate with one reg. set	Groups of 8	Priority by card location	
PRODUCTION	Date 1st delivery	5/69	12/66	4/68	12/68	4/68	12/68	5/66	10/68	6/67	8/69	
	Number installed	0	200	60	17	60	17	100	5	500	0	0
	Physical size	72 x 26 x 79	11 x 19 x 23	9 x 19 x 22	9 x 19 x 22	9 x 19 x 22	9 x 19 x 22	42 x 74 x 28	9 x 19 x 21	10 x 19 x 24FII	14 x 19 x 22	72 x 29 x 24
	Power	12kW 220V-2Ø	500	200	250	200	250	3kW 208V, 3Ø	300	340	850	1000
SOFTWARE	Compilers and systems	F, F IV in 8k	Basic F in 8kB, two assemblers, calculator	Maintenance	Maintenance, edit	Maintenance	Maintenance, math	F, operating system	Debug, maintenance test package	F IV, debug, diagnostics	ASA-F, I/O diagnostics	F IV * operating system*; assembler
OTHER FEATURES		• 4-sense switches • 2-port memory mods	• Character machine • Hardware bootstrap • Cabinet extra • Page size-256B.	• DTL & TTL IC's including MSI • Read only memory • 4-I/O slots	• DTL & TTL IC's • Disc avail. • Immune to noise	• DTL & TTL IC's including MSI • Read only memory • 4-I/O slots	• DTL & TTL IC's • Disc avail.* • Immune to noise	• Discrete logic • Hexadecimal • Operating temp. 70-80°F	• 2 independent sets of registers (including P) • Variable byte precision 1-4 • 3-sense switches	• Memory temperature servo • 3-sense sw. • Direct addressing to 32k	• Disc* • 16-sense • Maint. & prog. training • MSI & IC's	• Hardware square root • 4-sense switches • 24-bit switch register

PARAMETER \ COMPUTER		DDP 124	DDP 316	DDP 416	DDP 516	RC 70	DRC 44	DT 1600	EAI 640	G.A. 1830	HP 2114A	HP 2115A	HP 2116	IBM 1130
	Manufacturer	Honeywell				Redcor Corp.	Dynamics Research	Data Technology Corp.	E.A.I.	General Automation	Hewlett-Packard			International Business Machines
	Location	Framingham, Mass.				Canoga Park, Calif.	Wilmington, Mass.	Palo Alto, Calif.	Long Branch, N.J.	Orange, Calif.	Palo Alto, Calif.			
CLASS	Word size	24	16	16	16	16	24	8	16	16	16	16	16	16
	Cycle time	1.75	1.6	0.96	0.96	0.86	1.0	8.0	1.65	1.2	2.0	2.0	1.6	3.6
	Price	65.0	9.7	16.9	25.0	12.9	43.0	6.6	35.5	19.5	9.95	14.5	24.0	26
MEMORY	Basic size	8k	4k	4k	4k	4k	4k	4k	8k	4k	4k	4k	8k	4k
	Maximum size	32k	16k	32k	32k	32k	65k	16k	32k	32k	8k	8k	32k	32k
	Parity/protect	No	*/*	*/*	*/*	Yes/yes	*/Area*	No /*	No/yes	Yes/yes	*/no	*/no	*/*	Yes/No
INSTRUCTION SET	Number	48	72	30	72	35	78	73	64	32	70	70	70	29
	Multiply	14	5.3*	311-SW	5.3*	6.5*	12.0	SW	18	12.0	187-SW	24*-430FP*	19.2*	30-SW
	Indirect address					1								1
	Remarks	• Direct addressing 8k	• Hi-speed arith.* • Prepost indexing	• Add –1.92μs	• Prepost–indexing	• Relative addressing	• Direct add. 16k (6-index register)	• DP arith. • Direct to 512 words	• Rel. Addr. ±256 • DP • Prepost indexing	• Direct add. to 32k core • Base relative, indexed and indirect	Microprog. (up to 8 instructions per word)	• See 2114A • Protect disables last 64 locations	• See 2114A	• DP arith • Hexidecimal
REGISTERS	General	3A, 1X	2A, 1X	1A, 0X	2A, 1X	2A, 1X	2A, 6X	1	2A, 1X	16	2A	2A	2A	1, 2A, 3X
	Special		1(1)	–	1(1)	2	–	1	1	4	2	2	2	2(1)
	Total bits	96	70	16	49	70	192	9	48	320	34	34	34	98
I/O	Word rate	0.57	0.2	1.04	0.13-1.0	1.1	1.1	0.125	0.6	1.2	N.A.	0.5	0.625	0.45
	Channel types	MPX*, DMA*	MPX, SEL	MPX*, DMA*	DMA*, SEL, MPX	DMA, buffered transfer*	DMA, SEL, MPX	SEL, MPX*	Block transfers, DMA*	MPX, SEL, DMA	No DMA, MPX	DMA* (2 channels)	DMA, no MPX	Storage access channel
	Number of channels	0-4	1	1	1-4	1-64	3-8	1	1-2	1-6 (hi speed)	8	8-40	16-48	1
	Cycles stolen/word	1	–	1	1-4	1	1	1	1	–1	N.A.	1	1	1
	Sense lines	24 DL	16 DL	16 DL	16 DL	16 DL	24 DL	64		16 DL	16 DL	16 DL	16 DL	
	RT clock	*	*	*	*	60 Hz*	*	60 Hz*	Interval timer*	3 interval timers*	*	*	*	
	Price includes	300-Hz tape reader & punch	Console	ASR-33	ASR-33	Console	ASR-35	Console	Console	Console	Console	Console	Console	Console printer & keyboard
	Interfacing	• Option logic bloc • 20' cables • 4 DMA channels *	• 20 devices • Can use all 516 peripherals & interfaces	• 20 devices	• Simplex lines • Individually buffered I/O channel	• Party line • 8-device address lines	• 6-I/O inst. • Data bus allows additional processor units	• Party line • Interface to DTL & TTL	• Expanded input-18 bits from analog. • 64 external devices	• I/O bus line drivers & receivers* • Process I/O controller*	• Plug-in cards for peripherals • MPX* for 56 devices	• See 2114A	• 1-256 devices • 16 slots for plug-in cards	
INTERRUPTS	Number (min/max)	8-16	1-48	1-48	1-48	1-32	4-64	3-*	64	8-59	8-8	8-40	16-48	1-6
	Enable/disable	G/S	G/S group of 4	S	G/S group of 4	G/S	G/S	G/S	G/S	S	S	S	S	G/S
	Priority levels	16	1-48	48	1-48	Each int.	(4-64)*	3	64	0-61	Each int.	Each int.	Each int.	6
	Minimum service	6.3	2.88	2.88	2.88	1.7	3.3	8.0	5.8	1.32	8	4	3.0	14.4
	Power failure/restart	*/no	Yes/*	Yes/*	Yes/*	*/*	*/*	*/*	Yes/	Yes/yes	*/*	*/*	Yes/*	
	Remarks	–	–	Groups of 4	–			Groups of 8		6 internal interrupts			Assignment by card location	
PRODUCTION	Date 1st delivery	3/66	6/69	5/67	9/66	6/68	6/69	9/68	4/67	5/69	5/68	11/67	5/68	2/66
	Number installed	90	0	150	250	31	0	75	60	0	55	140	34	2600
	Physical size	13 x 26 x 24	19 x 25 x 14	24 x 24 x 38	24 x 24 x 38	19 x 19 x 19	19 x 16 x 22	9 x 19 x 22		16 x 19 x 22	12 x 17 x 25	12 x 17 x 25	31 x 16 x 20	46 x 58 x 29
	Power	2500	475	1400	1000	400	300	200	–	–	500-800	600-1200	1000-1600	1000-208V-1Ø
SOFTWARE	Compilers and systems	F IV, F DAP-II, DIP	F IV-8k, DAP, over 250 programs	DAP, diagnostics	F IV-8k, DAP, over 250 programs	F IV IN 8k, assembler in 4k	Diagnostic, I/O routines		F IV IN 8k, text editor	F, hardware test, real-time monitor exec., product control	Basic F; ALGOL, BASIC in 8k	Basic F; ALGOL, BASIC in 8k	Basic F, ALGOL, BASIC real-time exec.	Basic F
OTHER FEATURES		• Bootstrap • 6-sense sw. • Disc*	• 4-sense sw. • 4k of memory costs $5.5k • Logically identical with DDP 516 • 3 configurations avail.	• Disc* • Field upgrade to DDP 516.	• FP • 4-sense sw • Movable control console • Maint. & prog. training	• 8-sense sw. • Auto fill switch	• TTL IC's • Meets MIL-E-16400 • 3 hi-speed data channels standard	• Disc* • Mag. tape*	• Programming & maint. training • FP* • 8-sense sw. • Disc*	• Software compatible with IBM 1800-1130 • Wire-free & MSI • 13 control sw. • Alternate ROM* • Sys. I/O-$6k	• IC's-CTL, TTL • Rack-mountable • 1024-word page size • Protected controls • Prog. training	See HP 2114A	• IC's-CTL • Disc memory available* • Time-shared BASIC system • Programmer & maint.	• Internal disc of 516k words • Discrete logic

*Optional A–Accumulator X–Index B–Bytes F–Fortran P–Program counter PL–Party line I/O A FP–Floating point DP–Double precision

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	COMPUTER	IBM 1800	INTER-DATA 3	INTER-DATA 4	ITI 4900	LOCKHEED ELECTRONICS MAC 16	MDP 1000	MICRO 810	NOVA	PDP 8	PDP 12	PDP 15
	Manufacturer	IBM	Interdata		Information Tech., Inc	Lockheed Electronics	Motorola	Micro Systems	Data General	Digital Equipment Corp.		
	Location	–	Eatontown, N.J.		Sunnyvale, Calif.	Los Angeles, Calif.	Phoenix, Ariz.	Santa Ana, Calif.	Southboro, Mass.	Maynard, Mass.		
CLASS	Word Size	16	16	16	16	16	8	8	16	12	12	18
	Cycle Time	2.0	1.5	1.0	0.975	1.0	2.16	1.1	2.6	1.5	1.6	0.8
	Price	47	11.2	14.2	9.95	11.9	8.0	6.5	8.0	8.5	14.9	16.5
MEMORY	Basic size	4k	4kB	8kB	4k	4k	4k	4k	4k	4k	4k	4k
	Maximum size	32k	65kB	65kB	32k	65k	16k	32k	32k	32k	32k	128k
	Parity/protect	Yes/yes	*/yes	*/yes	*/*	*/*	No/no	*/*	No/no	*/no	No/no	*/*
INSTRUC-TION SET	Number	31	69	69	75	72	46	89	172*	28	43	79
	Multiply	16.2	Add-28 μs	Add-3.2 μs	10.0*	10*	SW	56-70 μs	300μ-SW	6.0*	9.0*	7.0*
	Indirect Address	1	No	No	∞	2	∞	∞	∞	1	1	1
	Remarks	• DP arith • Hexadecimal	• Microcode inst. operates at 0.37 μs • Mult./div.*	• Microcode inst. operates at 0.37 μs • Mult./div.*	• Microprog. • DP*	• 2 formats • Add-2μs • Mult./div*	• Add/sub. 4.32 μs • Automatic index incrementing	• Microprog. • 1, with ROM	• Add-5.9μ • Direct-addressing, 1024 words	• Can combine operations into single instruction	• See PDP 8L	• See PDP 8L
REGISTERS	General	2A, 3X	16	16	8 per program	1A, 1X	6, 3 may be used as X	15	4A	1A	1A	1A, 1X
	Special	2(1)	–	–	1 (1)	1	1 (3), 1 (1)	1	2A may be used as X	1 (1)	1 (1), 2(12),	1(1)1(9), 1(18)
	Total bits	82	256	256	129	17	64	128	64	13	37	124
I/O	Word rate	0.5	0.1B	0.15B	1.0	0.09-0.8	0.43	0.91	0.3	0.22-0.66	0.15-0.2	0.25-1.25
	Channel types	MPX, (2 types)	SEL, MPX*	SEL, MPX	SEL, MPX, DMA*	DMA*, MPX, prog.	DMA*	DMA* (2 channels)	DMA, SEL, MPX*	SEL, DMA	SEL, DMA	SEL, DMA
	Number of channels	3/9	1-16	16	0-256	1-16	12	0-32	1	0-7	1-14	8
	Cycles stolen/word	1	1	1	2	1	4 buffered memories*	1	1	3-1	3-1	3-1
	Sense lines	16 DL	16 DL	16 DL	16 DL	16 DL	12 DL	8 DL	16 DL	No	12	*
	RT clock	3-interval timers	60 Hz* or XTAL*	50 Hz* or XTAL*	Timer*	60 Hz	Relative time*	*	60 Hz* or XTAL*	*Several	*Several	*60 Hz
	Price includes	Console	ASR-33	ASR-33	Console	ASR-33	Console	Console	Console	ASR-33	ASR-33	ASR-33
	Interfacing	• D/A, A/D options	• A/D & D/A interface in 8, 10 or 12 bits • Drum with up to 8MB*	• A/D & D/A interface in 8, 10 or 12 bits • Drum with up to 8MB*	• Several types of adapters • 256 devices	• 255 devices • 5-I/O inst. • Party line	• Party line • Parallel I/O channel • Serial data interface for "Teletype"	• DTL byte-oriented I/O • 32 devices • 5-8 slots for plug-in interface	• TTL-IC logic levels • 62 devices • CRT* • 10-bit A/D & D/A conv.*	• Party line • Positive logic • 64 devices	• IC levels • 10-char./sec. tape read/punch • Many options prewired	• 256 devices • Data comm., A/D & D/A interfaces. • Party line
INTER-RUPTS	Number (min/max)	12-24	1-256*	1-256*	8-*	4-64	1-64	2-64	1-62	1	1	1-92
	Enable/disable	G/S	S	S	G/S	G/S	G/S group of 8	G/S	S	S	S	S
	Priority levels	24 levels	256	256	Each unique	4-64	Each int.	64	16	1	1	8
	Minimum service	2.25	23	18	6.0	6.0	24.0	9.9	4.4	4.8	4.8	0.8
	Power Failure/restart	Yes/no	Yes/yes	Yes/yes	*/*	*/*	*/*	*/*	*/*	*/*	*/*	*/*
	Remarks	—	—	—	Groups of 8	Expandable in groups of 4	Programmable levels	Groups of 8	16 programmable levels			
PRODUC-TION	Date 1st delivery	2/66	3/67	8/68	6/65	2/69	1/68	1/69	2/69	11/68	5/69	10/69
	Number installed	450	150	55	20	20	40	25	7	4500	–	0
	Physical size	68 x 33 x 76	15 x 19 x 21	90 x 22 x 27	19 x 19 x 22	18 x 17 x 21	6 x 17 x 21	9 x 19 x 23	5 x 19 x 22	9 x 19 x 21	71 x 33 x 35	70 x 30 x 28
	Power	5000-208V-3Ø	300	300	400-900	500	60	340	400	250	2000	1500
SOFT-WARE	Compilers and systems	Basic F, time-shared exec., operations monitor, MPX	F, in 8k, debug	F, debug	Symbol, math, operating system, F IV in 8k	F IV in 8k, exec, editor, diagnostics	Mult. precision arith. code conv.	F, diagnostics, debug	Debug, utility, FP	BASIC, FOCAL, utility, F, F IV in 8k, ALGOL	F, BASIC, FOCAL ALGOL	COMPACT, F IV,
OTHER FEATURES		• Discrete logic • Control & data path for attachment to System/360 • Disc-512k*	• 16-sense sw. • 16 registers reside physically in core • FP* • Prog. & maint. training		• Disc* • 100% tested by another ITI 4900	• TTL-IC's • Remotable control panel • Prog. & maint. training • Disc systems* • 4 memory index registers	• Wirefree • TTL logic • 12-bit inst. words. • Analog digital, & interface I/O modules*	• 220-ns ROM. 256 words min., 1024 words max. • TTL and MSI-IC's • Mother board const.	• MSI • Read only* memory • Incremental plotter*	• SW compatible with PDP 5, 8, 12 • 8 auto index • 12-sense sw. • Extensive documentation	• SW compatible with PDP 5, 8, line • 15 auto-index registers • 6-sense sw. • Succeeds Line-8	• 512k disc* • SW compatible with PDP 4, 7, 9 • Auto-index • Extensive documentation

	COMPUTER	RAYTHEON 703	RAYTHEON 706	SCC 660	SCC 4700	SDS CE16	SDS CF16	SEL 810A	SEL 810B	SEL 840MP	SIGMA 2	SPC 12	SPIRAS 65	TEMPO I
	Manufacturer	Raytheon		Scientific Control Corp.		Scientific Data Systems		Systems Engineering Labs.			Scientific Data Systems	General Automation	IRA Systems	Tempo Computer
	Location	Santa Ana, Calif.		Dallas, Tex.		El Segundo, Calif.		Fort Lauderdale, Fla.			El Segundo, Calif.	Orange, Calif,	Waltham, Mass.	Orange, Calif.
CLASS	Word Size	16	16	24	16	16	16	16	16	24	16	8	16	16
	Cycle Time	1.75	0.9	1.75	0.92	8.0	2.63	1.75	0.75	1.75	0.9	216	1.8	0.9
	Price	15.0	19.0	27.0	16.2	12.8	14.9	18.0	30.0	60	26	5.0	14.9	15.6
MEMORY	Basic size	4k	4k	4k	4k	4k	4k	4k	8k	8k	4k	4k	4k	4k
	Maximum size	32k	32k	32k	32k	16k	16k	32k	32k	98k	65k	16k	65k	65k
	Parity/protect	No/no	*/area	Y/area	*/*	No/no	No/no	*/*	Yes/*area	Yes/*	Yes/*	No/no	*/yes	*B/*
INSTRUC-TION SET	Number	74	74	59	98	126	126	55	55	65	37	50	200	100
	Multiply	14*	8.0*	14.0	8.44	126-SW	126-SW	7.0	4.5	10.5	10.35*	SW	17.0	5.8*
	Indirect Address	No	No	∞	1	∞	∞	∞	∞	∞	2	1	∞	1
	Remarks	• 2048-word pages	• 2048-word pages	• Instr. decoded in ROM. May add special instr, DP or FP • Relative address ±256		• Relative addressing ±256 • 16 memory reference instructions		• Privileged instructions* • Variable-base register	• Privileged instructions* • Protection in 512-word pages	DP* in extended arith. unit.	• Hexadecimal • Protect for 256-word pages	• Add-6 μs • Relative addressing ± 256	• ROM-32 x 512 • Relative addressing ±511 • DP + FP	• Floating page • Add-FP-30 μs • DP
REGISTERS	General	1A, 1X	1A, 1X	2A, 1X	2A, 1X	2	2	2A	2A, 2X, (1*)	2A, 3X	2A, 2X	1A, 3X	2A, 1X	8-16
	Special	1 (5)	1 (5)	2 (1)	2 (1)	–	–	–	–	4-4	–	1	–	3
	Total bits	37	37	74	50	32	32	32	32	109	64	49	48	304
I/O	Word rate	0.07-0.57	0.14-1.1	0.19-0.57	0.09-0.91	0.025-0.125	0.068-0.187	0.2-0.57	0.3-1.3	0.2-0.57	0.4B	0.46	0.1-0.5	0.90-0.7
	Channel types	DMA*	DMA *	DMA	All	SEL, DMA*	SEL, DMA*	SEL	SEL	DMA, SEL	MPX, DMA*	DMA*, SEL	MPX, DMA*	SEL, DMA*
	Number of channels	6	6	1-3	0-4	4	4	0-8	0-8	*-6	4-20	0-1	1-2	1
	Cycles stolen/word	1	1	1-4	0-3	1-4	1-4	1	1	1	1	1	5	1
	Sense lines	–	–	*	16-256	16 DL	16 DL	16 DL	16 DL	24 DL	16 DL	12 DL	–	16 DL
	RT clock	*	*	*60 Hz	60 Hz	*	*	60 Hz*	60 Hz*	60 Hz*	4 types*	Yes	*	*
	Price includes	ASR-33	ASR-33	ASR-35	Console	ASR-33	ASR-33	ASR-33	ASR-33	ASR-33	ASR-35	TTY interface	Console	ASR-33
	Interfacing	• 256 devices • Analog* • PL to 50' • Simplex lines	• 256 devices • Analog* • PL to 50' • Simplex lines	• Simplex lines • Up to 256 channels	• Simplex lines • 64 devices per channel • Extensive options	• 32 I/O devices, 8 functions per device • Disc* & drum*		• 16-256 devices • Party line • Auto. block transfer control units	See 810A	• 16-64 PL • 8-block transfer control units • CRT* • Disc*		• Duplex, 2000 foot lines • 2 I/O instructions • 6 sets of I/O interface mod-	• PL to 63 dev • 4 I/O controllers. • DTL/TTL logic levels	• 64 devices • I/O DTL compatible • Byte transfer*
INTER-RUPTS	Number (min/max)	1-16	1-16	2-64	2-256	3-*	3-**	2-96	2-98	3-60	3-132	1-9	1	4-256
	Enable/disable	S	S	S	G/S group of 16	G	G	G/S group of 12	G/S group of 12	G/S group of 16	G/S group of 16	S	S	G/S group of 16
	Priority levels	1-16	1-16	1-64	2-18	Priority hardwired		Each int.	Each int.	Each int.	Each unique	Each unique	By device number	1-16
	Minimum service	5.25	2.7	5.2	7.36	8.0	2.63	5.2	2.2	5.2	4.0	4.3	5.4	3.6
	Power Failure/restart	*/*	*/*	*/no	*/*	*/*	*/*	Yes/yes	Yes/yes	Yes/yes	*/*	*/*	*/*	*/*
	Remarks	Groups of 4	Groups of 4	Groups of 8	Registers are auto saved	Third interrupt is expandable to "n" devices		–	–	–	Parity int.*	Expander unit*	Int. source number on I/O bus	–
PRODUC-TION	Date 1st delivery	10/67	2/69	6/66	2/69	7/69	9/69	8/66	10/68	1/68	12/66	12/67	6/69	8/69
	Number installed	110	12	110	20	0	0	110	14	10	60	150	0	0
	Physical size	11 x 17 x 20	11 x 17 x 20	108 x 19 x 21	64 x 31 x 36	9 x 19 x 22	9 x 19 x 22	24 x 62 x 26	24 x 62 x 30	72 x 53 x 27	≈24 x 50 x 30	5 x 18 x 20	14 x 19 x 26	53 x 18 x 22
	Power	690	900	6k	2k	250	250	1200	1200	3500	1500	–	–	60-400
SOFT-WARE	Compilers and systems	F IV in 8k, real-time operation system	F IV in 8k, real-time operation system	F, assembler, diagnostic	F IV in 8k, F	F in 4k, diagnostics		F IV in 8k, F library, maint.	F IV in 8k, real-time exec.	F IV, real-time monitor	F, F IV, 2 operating systems	F II	F IV – 8k, bootstrap loader	F IV in 8k, hexidecimal mnemonics, maint. prog.
OTHER FEATURES		• Byte & word addressing • Disc-400,000 words* • Buffered digital channels	• Hardware bootstrap • Console lockout • 4-sense sw.	• Programmer & maint. training	• 4-port memory modules • Communication options • TTL-IC's • 16-sense switches	• TTL & DTL-IC's • Automatic I/O instruction, DMA. • Three-way compare (3 skips) • Machines marketed as controllers by module div. • OEM is Computer Automatic Corp.		• 16-sense sw. • Disc*-1,024,000-word capacity	• 16-sense sw. • 15-bit program counter	• 4-sense sw. 20-sense sw.* • 4-4-bit page registers, page 8k words • Multi-process options	• Rapid-access data-3,000,000 bytes	• 8-bit memory • 12-bit CPU • 24V DC adapter 4. Wire-free construction	• "Nixie" register display • 4-sense sw. • 12-bit A/D-D/A • IRA scope*	• 4-sense sw. • Bootstrap loader* • TTL & MSI • Remote console*

*Optional A–Accumulator X–Index B–Bytes F–Fortran P–Program counter PL–Party line I/O FP–Floating point DP–Double precision

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